to the main-gate reduction. Thus, the condition of the same side-gate length as that of the main-gate promises good device operation including immunity to the short channel effect. The simulated peak

substrate currents are shown to provide saturation current in Fig. 3. The side-gate MOSFET in the LSG of 50 nm shows the improvement in the drain saturation current without a severe substrate current increase due to hot carrier effects as the side-gate bias increases [4].

Fig. 2 Vf roll-off and DIBL characteristics

- VGS=1.0 V
- VGS=1.5 V
- VGS=2.0 V

Fig. 3 Peak substrate current characteristics

- simulation
- experiment

Device fabrication and characterization: The side-gate MOSFET fabrication process is based on conventional MOS technology. After active area definition, the channel region was implanted with B⁺ and BF² for the purpose of punch-through stop and Vf adjustment. The sidewall patterning technique [5], the side- and inter-gate oxide growth, and n-type poly-Si etch-back is different from conventional methods. The sidewall patterning technique was adopted to realise a 50 nm poly-Si line as the main-gate electrode as shown in Fig. 1b. The side- and inter-gate oxide growth was simultaneously carried out using oxidation rate difference between the doped poly-Si and the bulk Si surface. After the side- and inter-gate oxidation process, poly-Si etch-back for the formation of side-gates is performed as shown in Fig. 1c. At the end of the process, Al with 1% Si is used for the metallisation without alleviation. Fig. 4 shows the transfer characteristics in the side-gate MOSFET with a main- and side-gate length of 50 nm and 50 nm. As shown in this figure, a small DIBL of 77 mV, a maximum transconductance (gmax) of 120 μS/μm, and a good subthreshold swing (SS) of 81 mV/dec is clearly observed in the 50 nm gate condition. The fabricated device has a threshold voltage of 0.091 V in agreement with simulation results.

Conclusions: 50 nm long MOSFETs with additional side-gates were characterised in terms of performance dependency on the side-gate length and successfully fabricated with conventional MOS technology. The device simulation results reveal that the device can show optimal transistor operation when the side-gate length is equal to the main-gate. A side-gate MOSFET fabricated using this design guideline shows normal transistor operation including reasonable switching and short channel and hot carrier effects characteristics.

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References


Dynamic exclusive-OR gate based on gate-induced Si island single-electron transistor

Dae Hwan Kim, Kyung Rok Kim, Suk-Kang Sung, Jong Duk Lee and Byung-Gook Park

Basic operation of a dynamic exclusive-OR gate implemented by a field effect transistor and a single-electron transistor is experimentally demonstrated, for the first time. Logic output voltage shows full swing operation at a supply voltage of 20 mV. Fabricated single-electron transistors are advantageous for implementing a multi-gate single-electron logic circuit.
Introduction: Single-electron transistors (SETs) have recently attracted much attention as a candidate for ultra-high density, low power nanoelectronic devices, because their operation is based on the Coulomb blockade in a nanostructure and performs at a very low supply voltage. However, since there are inherent limitations in the application of SETs (low driving current and low voltage gain) in the conventional circuit scheme, it is a challenge to implement their advantages into a chip for better performance as a total system. This implies that the most realisable system in the near future is the metal-oxide-semiconductor field effect transistor (MOSFET)-SET hybrid circuit [1]. Consequently, a fabrication technique for SETs compatible with the conventional MOS process technology is strongly required, for the purpose of integration with conventional MOSFETs. We have developed a fabrication technique for SETs based on the gate-induced Si island by the combination of conventional photolithography and process technology [2].

Conversely, an exclusive-OR (XOR) gate is the basic element of a full adder which comprises an arithmetic logic unit, and it is conventionally composed of six transistors. The feasibility of a XOR gate based on multi-gate SETs has been already demonstrated [3], but its signal was limited by the SET current.

We report the experimental demonstration of a dynamic XOR gate composed of only two transistors i.e. one MOSFET and one SET, for the first time, in this Letter. Since their depletion gates can control the peak position of the Coulomb oscillation, SETs used in an XOR gate are advantageous for the implementation of a multi-gate SET logic circuit.

Device structure and characteristics: The starting material was a 4 × 10^{17} cm^{-3} p-type 45 nm thick top layer of a silicon-on-insulator (SOI) [100] wafer prepared by separation by implanted oxygen. This top layer was separated from the Si substrate by 415 nm thick buried oxide. SETs with sidewall depletion gates on an SOI nanowire were fabricated, using a combination of conventional lithography and process technology. The key fabrication technique consists of two sidewall process techniques, which are the patterning of a uniform SOI nanowire by the sidewall patterning method [2] and the formation of n-doped polysilicon sidewall depletion gates. More detailed information about the fabrication was reported elsewhere [2]. Fig. 1a shows the schematic diagram of the device structure. The electron channel in an SOI nanowire is formed by the back gate voltage, \( V_{BG} \), and two tunnel junctions are formed by the sidewall depletion gate voltage, \( V_{SG} \). The potential of the gate-induced Si island is controlled by the control gate voltage, \( V_{CG} \). Fig. 1b and c show the cross-sectional diagram of the device and the equivalent circuit diagram. In addition to tunnel junction formation, the \( V_{SG} \) can control the peak position of the Coulomb oscillation due to sharing of the gate-induced island charge between the control gate and the sidewall depletion gate, as shown in Fig. 2.

![Image 1](image1.png)

**Fig. 1** Schematic diagram and equivalent circuit of fabricated SET

(a) Schematic diagram of fabricated SET

- \( W_{CG} = 30 \) nm, \( T_{SOI} = 60 \) nm, \( T_{SOI} = 140 \) nm, \( W_{SOI} = 30 \) nm

- Cross-sectional view of fabricated SET and voltage notations

(b) Equivalent circuit of fabricated SET when back gate voltage, \( V_{BG} \), is fixed

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![Image 2](image2.png)

**Fig. 2** Sidewall gate voltage dependence of Coulomb oscillation peak position

\( V_{G0} = 20 \) mV, \( V_{BG} = 4 \) V, \( T = 8 \) K; 'HIGH' corresponds to 70 mV

![Image 3](image3.png)

**Fig. 3** Equivalent circuit diagram of dynamic two-input XOR logic gate

**Experimental dynamic two-input XOR gate:** On the basis of the current peak position control by the sidewall depletion gates, we propose a dynamic two-input XOR gate composed of a MOSFET and a SET. Fig. 3 shows the circuit diagram of the proposed XOR gate, where the MOSFET switched by \( V_{CLK} \) is utilised as the pull-up device and the SET switched by \( V_{CG} \) and \( V_{SG} \) as the pull-down device. When compared with the static CMOS-type SET logic [4], the concept of the dynamic SET logic [5] is more promising, because the inherent drawback of low voltage gain becomes less conspicuous. Moreover, this approach is very desirable and suitable for our SETs, because the compatibility with conventional MOS technology is the prominent merit of our fabrication method [2]. The load capacitance, \( C_L \), is charged up to 20 mV during the precharge period, and the evaluation is performed during the OFF period of the MOSFET as shown in...
Fig. 4a, Fig. 4b and c show the waveforms of two input voltages, \( V_{\text{CG}} \) and \( V_{\text{FS}} \), synchronised with \( V_{\text{CLK}} \). During four periods of evaluation, four different binary combinations of \( V_{\text{CG}} \) and \( V_{\text{FS}} \) are accommodated by two input voltages. Although the voltage levels of input and output are mismatched, the waveform of the output voltage shows full swing XOR operation with respect to the supply voltage, \( V_{\text{DD}} \), as shown in Fig. 4d.

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### References

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### Enhanced intersubband absorption in stepped double barrier quantum wells

K.T. Lai, S.K. Haywood, R. Gupta and M. Missous

Intersubband absorption is measured in the conduction band of GaAs and stepped GaAs/InGaAs. As multiple-quantum-wells confined by narrow AlAs barriers. Enhanced absorption from \( n=1 \) to \( n=2 \) is observed in the stepped wells. This is attributed to relaxation of the intersubband population selection rule.

**Introduction:** Two windows in the atmospheric absorption spectrum can be exploited for the optical detection of gases. In the long-wavelength window from 8-12 \( \mu \)m, quantum well intersubband photodetectors based on lattice-matched GaAs/AlGaAs as wells provide high performance detector elements [1]. The choice of detector is less clear for the 3-5 \( \mu \)m window, where gases such as CO, CO2, and CH4 exhibit well resolved vibrational absorption bands [2]. To achieve an intersubband transition in GaAs/AlGaAs quantum wells (QWs) below 5.6 \( \mu \)m requires indirect AlGaAs barriers i.e. \( x>0.45 \). Beyond the \( T-\Delta E \) crossover the thermal activation energy is reduced and therefore device dark current increases [3]. In addition, the \( T-\Delta E \) scattering associated with \( x>0.45 \) together with GaAs X-barrier trapping can result in inefficient carrier collection and thus a decrease in photocurrent. Nevertheless, the mature epitaxial growth and processing technology of GaAs-based materials leads to high growth uniformity and excellent reproducibility. Thus despite the problems associated with indirect barriers, it may still be desirable to use GaAs/AlGaAs as intersubband detectors in this wavelength region. Thus indirect AlAs barriers in combination with GaAs or strained InGaAs wells have been shown to be effective in enhancing the responsivity of 3-5 \( \mu \)m intersubband transitions due to improved carrier confinement [4, 5]. Stepped QWs are also known to relax the selection rules for intersubband transitions [6]. In this Letter we present a comparative study of the intersubband absorption of square and stepped wells in a double barrier quantum well (QBW) structure i.e. the QW is confined by thin AlAs and wide direct Al,Ga,As barriers.

![Fig. 1 Modelled conduction band-edge profile for sample 1557](image_url)

**Sample details:** The samples were grown by molecular beam epitaxy on a (100) semi-insulating GaAs substrate in a VG Semicon V90H reactor with 4 in substrate growth capability. We used near-stoichiometric growth conditions [7] at low temperatures (~250°C) to achieve the high optical quality evidenced by efficient room temperature photoluminescence from all the samples. Table 1 shows the detailed sample parameters. Each sample has 50 well/barrier periods in the active region sandwiched between a 10 nm undoped GaAs cap layer and a 100 nm undoped GaAs buffer layer. The wells are confined by 2 nm AlAs barriers followed by 22 nm Al0.5Ga0.5As. Samples 1546 and 1551 both have 4.5 nm GaAs wells of different silicon doping level. Sample 1557 is a stepped InGaAs well where only the InGaAs layer is doped. Fig. 1 shows the conduction band-edge

<table>
<thead>
<tr>
<th>Sample No.</th>
<th>InGaAs (% In)</th>
<th>Well width (nm)</th>
<th>( N_d ) ( \times 10^{14} \text{cm}^{-2} )</th>
<th>( N_s ) ( \times 10^{11} \text{cm}^{-2} )</th>
<th>Absorption peak (( \mu )m)</th>
</tr>
</thead>
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<tr>
<td>1546</td>
<td>0</td>
<td>0.5</td>
<td>1.7</td>
<td>7.7</td>
<td>3.62</td>
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<td>1551</td>
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<td>2.4 + 2.4</td>
<td>8.5</td>
<td>20.4</td>
<td>3.70</td>
</tr>
<tr>
<td>1557</td>
<td>25</td>
<td>2.4 + 2.4</td>
<td>8.5</td>
<td>20.4</td>
<td>3.70</td>
</tr>
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</table>