# Effect of Nitrogen Content in Tunneling Dielectric on Cell Properties of 3-D NAND Flash Cells

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***Abstract*—The effect of band engineering by controlling nitrogen content in the tunneling dielectric of the 3-D NAND flash cells is investigated by comparing various cell properties of the two devices. These measured devices have the same device dimensions and different nitrogen contents. The device with higher nitrogen content shows larger trap density profile and improved erase characteristics. After the same P/E cycling stress, the device with higher nitrogen content shows larger increase of trap density and more significant degradation in its erase characteristics. The electrons stored in the device with higher nitrogen content more easily escape through the trap-assisted tunneling mechanism due to higher trap density, resulting in worse retention characteristics at room temperature.**

***Index Terms*—3-D NAND flash memory, tunneling dielectric, band engineering, interface trap density.**

## I. Introduction

RECENTLY, 3-D NAND flash memory with vertical bit-line (BL) has become a mainstream in the industry to obtain higher memory density and smaller bit cost [1]–[4]. In the structure based on bit-cost scalable (BiCS) technology, poly-Si body is separated from the substrate [4], so no holes can be supplied to the poly-Si body from the substrate during erase operation. So, Gate Induced Drain Leakage (GIDL) mechanism should be used to generate holes in the body in erase operation [5]. In order to improve erase characteristic without the structure change, band engineering can be applied to tunneling oxide [6], [7]. However, since the band engineering changes the dielectric property, it is necessary to study its effect on the cell characteristics. Previous studies about effects of band engineering have focused on hole/electron tunneling rate through the tunneling dielectric, program/erase (P/E) characteristics, gate leakage current, and oxide breakdown charge [6]–[10]. In particular, such studies have been mainly investigated in planar MOS devices, which have different channel material, device dimension, structure, and operation condition from those of 3-D NAND flash memory.

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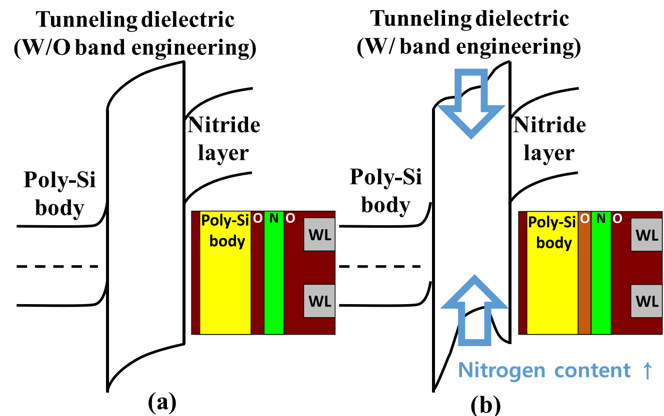


Fig. 1. Energy band diagrams along the WL direction of 3-D NAND flash memory cell, (a) without and (b) with band engineering in tunneling dielectric.

In this letter, we investigate the effect of the band engineering on the 3-D NAND flash memory cell properties. To compare the trap characteristics, we extract the trap density in wide-range of energy level from capacitance and conductance characteristics by utilizing conductance method [11], [12]. In order to analyze the effect of band engineering on the P/E characteristics, threshold voltage ($V_{th}$) shift is observed with increasing step pulses. The effect of cycling stress on the cell characteristics is explained by comparing trap density profiles and P/E characteristics of the cells before and after the P/E cycling stress. At last, retention characteristics are compared.

## II. Theory and Measurement Method

Fig. 1 shows energy band diagrams of the 3-D NAND flash memory cells along the word-line (WL) direction without and with the band engineering. As shown in the Fig. 1 (b), band structure of the tunneling dielectric is changed by band engineering. This energy band change is more pronounced at the valence energy than at the conduction energy due to bandgap and affinity difference between oxide and nitride [6], [7]. The degree of the change becomes larger with increasing nitrogen content.

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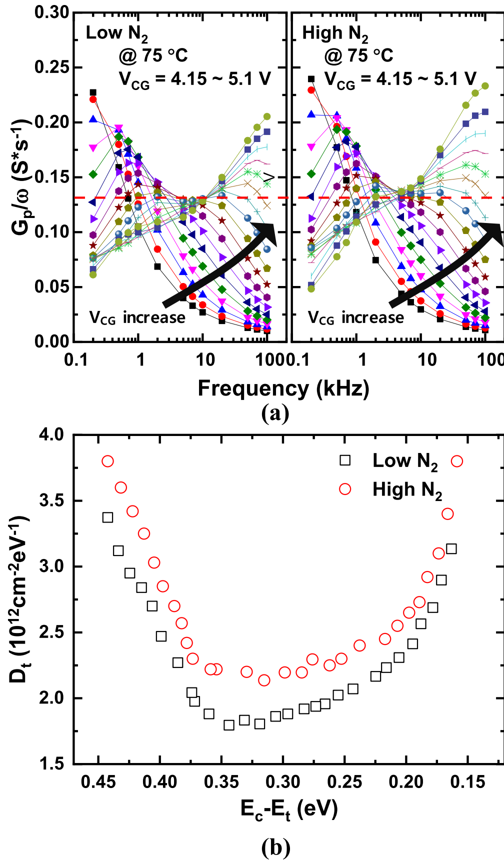


Fig. 2. (a) $G_p/\omega$ curves of low and high $N_2$ samples at 75 °C. (b) Extracted $D_t$ profile of low and high $N_2$ samples as a parameter of trap energy level.

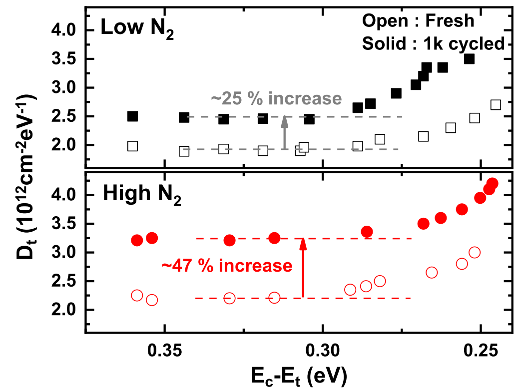


Fig. 3. Extracted $D_t$ profile of the low and high $N_2$ samples in the energy range of 0.25 ~ 0.4 eV before and after 1k P/E cycles.

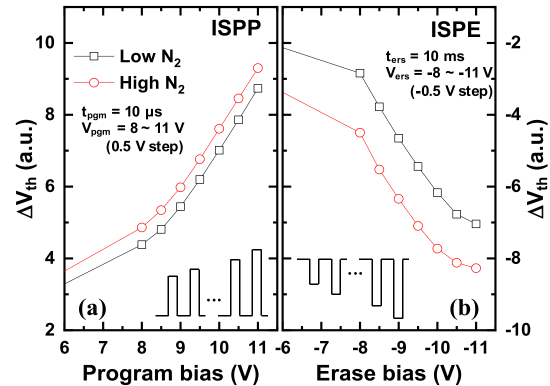


Fig. 4. $\Delta V_{th}$ of low and high $N_2$ samples by (a) ISPP and (b) ISPE. Insets show increasing step pulse waveform used in the measurements.

In order to investigate the effect of the band engineering, we measured two 3-D NAND flash memory devices fabricated in the industry [3]. These two devices have the same device dimensions and fabrication process except $N_2$ concentration in atmosphere during the tunneling dielectric fabrication process. These two devices are named low and high $N_2$ samples, depending on nitrogen content.

## III. Results and Discussion

### A. Trap Characteristics

Fig. 2 shows parallel conductance over frequency ($G_p/\omega$) curves and extracted trap density ($D_t$) profiles of low and high $N_2$ samples by utilizing conductance method [12]. As shown in Fig. 2 (a), peak values of $G_p/\omega$ curves of high $N_2$ sample at each control gate bias ($V_{CG}$) are larger than that of low $N_2$ sample. It results in higher $D_t$ of the high $N_2$ sample as in Fig. 2 (b). The $D_t$ of the high $N_2$ sample is about 18 % larger than that of the low $N_2$ sample at energy level between 0.25 ~ 0.4 eV. This larger $D_t$ in the high $N_2$ sample is caused by excess nitrogen atoms which cause oxide internal stress and larger trap origins [13], [14].

During the P/E cycle, traps are generated due to repeated F-N tunneling [15]–[17]. After the 1k P/E cycles, these generated traps are observed as increased $D_t$ as in Fig. 3. About 25 % and 47 % of $D_t$ increase are observed in the low and high $N_2$ samples. This larger trap generation of the high $N_2$ sample with the same cycling stress is due to the greater mechanical stress in dielectric due to excess nitrogen atoms [13].

### B. Program/Erase (P/E) Characteristics

Fig. 4 shows $V_{th}$ shift ($\Delta V_{th}$) by P/E biases with the increasing step (ISPP/ISPE). The insets show pulse waveform used in ISPP/ISPE. The high $N_2$ sample shows larger $\Delta V_{th}$ because the band offset during P/E operation is more significant in the high $N_2$ sample due to larger band structure change. Moreover, since larger band offset occurs at valence band than at conduction band, erase characteristics shows larger improvement [6], [7]. Note that the slopes of ISPP/ISPE characteristics of the both samples are almost the same since the both samples are charge trap flash device [18].

Fig. 5 shows ISPP/ISPE characteristics of the two samples before and after 3k P/E cycles. In P/E cycling, the bias for one pulse is set to provide the same $\Delta V_{th}$ in each sample. After the P/E cycles, P/E characteristics of the samples are changed due to buildup of trapped electrons in the devices [16]. In the ISPP measurement, both samples show about 4 % of $\Delta V_{th}$ increase after the 3k P/E cycles. On the other hand, in the ISPE measurement, $\Delta V_{th}$ of the low $N_2$ sample shows about 9 % decrease after 3k P/E cycles on the while that of the high $N_2$ sample shows about 15 % decrease. Larger deterioration in the erase operation of high $N_2$ sample is due to the higher amount of trap generation and trapped electrons caused by excess nitrogen in the tunneling dielectric bulk [19], [20].

### C. Retention Characteristics

Fig. 6 shows retention characteristics of the low and high $N_2$ samples at 25 °C and 75°C. The high $N_2$ sample shows larger

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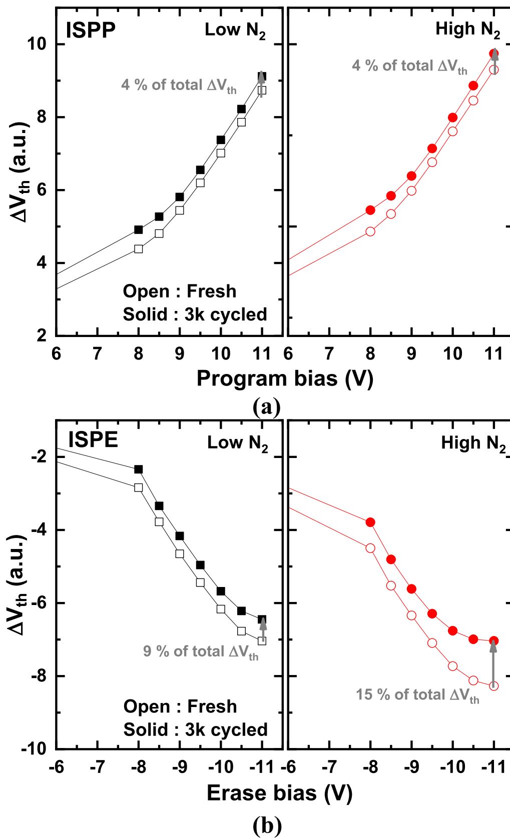


Fig. 5. $\Delta V_{th}$ of low and high $N_2$ samples by (a) ISPP and (b) ISPE, before and after 3k P/E cycles.

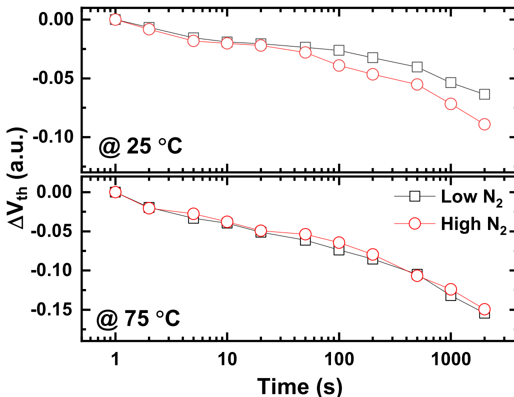


Fig. 6. $V_{th}$ shift of low and high $N_2$ samples at 25 °C and 75 °C for 2000 seconds.

$\Delta V_{th}$ at 25 °C than the low $N_2$ sample while two samples show similar $\Delta V_{th}$ at 75 °C. At 75 °C, electron escape by thermal emission mechanism is dominant so that effect of TAT can be ignored [21], [22]. Since the two samples have the same device dimensions and fabrication process except the nitrogen content in the tunneling dielectric, the amount of electrons escaped by thermal emission is similar, resulting in similar $\Delta V_{th}$ at 75 °C. On the other hand, the effect of TAT term cannot be ignored at 25 °C and larger trap density in high $N_2$ sample results in larger $\Delta V_{th}$ at 25 °C.

## IV. Conclusion

In this work, we have studied about effect of nitrogen content in tunneling dielectric on cell reliability of 3-D NAND flash memory. The cell which has higher nitrogen content showed larger trap density and better erase characteristics compared to the cell with lower nitrogen content. When the same P/E cycling stress was applied to both samples, larger increase in trap density and a more severe erase characteristics degradation were observed in the cell with higher nitrogen content. In addition, it was shown from measured retention characteristics that a larger amount of electrons escapes from the storage layer of the cell with higher nitrogen content through the trap assisted tunneling mechanism. These results demonstrate that band engineering by controlling nitrogen content in the tunneling dielectric leads the advantage in erase characteristics but also leads poor P/E cycling endurance.

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