A Practical SPICE Model Based on the Physics and Characteristics of Realistic Single-Electron Transistors

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***Abstract*—A practical model for a single-electron transistor (SET) was developed based on the physical phenomena in realistic Si SETs, and implemented into a conventional circuit simulator. In the proposed model, the SET current calculated by the analytic model is combined with the parasitic MOSFET characteristics, which have been observed in many recently reported SETs formed on Si nanostructures. The SPICE simulation results were compared with the measured characteristics of the Si SETs. In terms of the bias, temperature, and size dependence of the realistic SET characteristics, an extensive comparison leads to good agreement within a reasonable level of accuracy. This result is noticeable in that a single set of model parameters was used, while considering divergent physical phenomena such as the parasitic MOSFET, the Coulomb oscillation phase shift, and the tunneling resistance modulated by the gate bias. When compared to the measured data, the accuracy of the voltage transfer characteristics of a single-electron inverter obtained from the SPICE simulation was within 15%. This new SPICE model can be applied to estimating the realistic performance of a CMOS/SET hybrid circuit or various SET logic architectures.**

***Index Terms*—MOSFET, realistic single-electron transistor, single-electron inverter, SPICE model.**

I. Introduction

MOTIVATED by the merits of density, power, and functionality, various structures of single-electron transistors (SETs) have been recently demonstrated. From the viewpoint of the new functionality of SETs such as the CMOS/SET hybrid circuit system, the development of a simulation scheme using a conventional circuit simulator is an emerging challenge. While the previously reported simulation techniques were based on a numerical calculation of a master equation or a Monte Carlo method [1]–[4], these methods are often time-consuming, and cannot be easily expanded to a CMOS/SET hybrid circuit. Macro-model [5] and analytical SET models [6] for conventional SPICE simulators have recently been proposed and successfully verified in terms of their usefulness and accuracy. Nevertheless, these models are unsatisfactory for analyzing and optimizing the performance of SETs in a real chip, because they are validated by a comparison with the Monte Carlo simulation results rather than actual experimental data.

In this study, a practical SPICE model based on the physical phenomena in realistic Si SETs was developed, and implemented into a conventional SPICE circuit simulator. The SPICE simulation results were compared with the measured characteristics of Si SETs. The distinctiveness of our model is that a single set of model parameters is used, while still considering divergent physical phenomena such as the parasitic MOSFET, the Coulomb oscillation phase shift, and tunneling resistance modulated by the gate bias. Secondly, estimation of the model parameters is intuitively possible, because this model begins from the analytic model, and includes the physical meaning of its parameters. The paper is ordered as follows. In Section II, the geometrical structure and electrical characteristics of the fabricated SETs, which are reported elsewhere [7], [8], are briefly reviewed. In Section III, the details in implementing the physical phenomena and structure of the realistic SETs are presented. Finally, the SPICE simulation results of our model are compared with the experimental characteristics of the Si SETs and the reliability of our model is confirmed in Section IV.

II. Device Structure and Electrical Characteristics

Fig. 1 shows a schematic diagram of the device structure and cross section of the SET with sidewall depletion gates on an silicon-on-insulator (SOI) nanowire [7]. An electrically induced Coulomb island is formed in the 30-nm-wide channel ($W_{\rm ch}$) of the SOI MOSFET by the field effect of the sidewall depletion gate bias. This device shows good controllability and reproducibility over a wide range of temperatures (4.2 K$\sim$77 K). Detailed information about its fabrication is reported elsewhere [8]. In particular, the island size ($S_{\rm sg}$) is split in the range of 40$\sim$190 nm with the aim of controlling the electrical behavior of the SETs. This allows the size of the island to be considered as a design parameter, which can further optimize the performance of SET logic circuit. For example, the logical "HIGH" voltage is given by half the period of the Coulomb oscillation in most SET logic circuitry.

Fig. 2 shows the electrical characteristic of the fabricated SETs. While the Coulomb oscillation is shown with a sweeping control gate voltage ($V_{\rm cg}$), three physical phenomena that are

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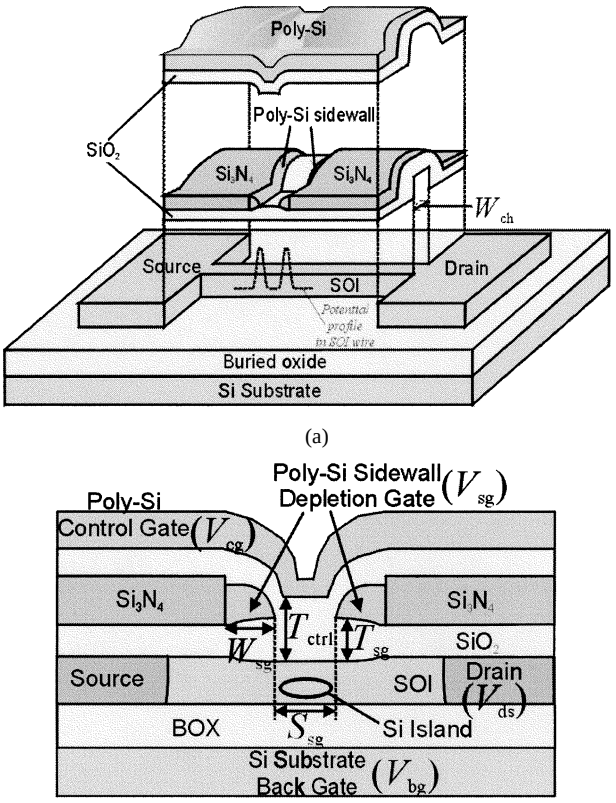


Fig. 1. (a) Schematic diagram of the fabricated Si SETs with sidewall depletion gates and (b) cross-sectional view of (a). Here, the island size $S_{\rm sg}$ can be controlled over the range 40–190 nm.

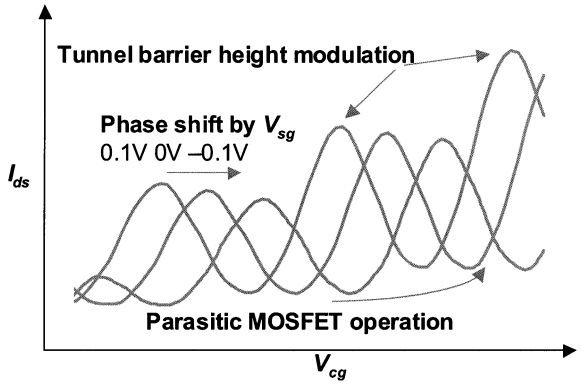


Fig. 2. Typical electrical characteristics of the fabricated SETs. The device with an island size $S_{\rm sg} = 40$ nm was measured at 77 K ($V_{\rm ds} = 5$ mV and $V_{\rm sg}$ ranges from -0.1 to 0.1 V).

distinguished from the *orthodox theory* are clearly observed in the realistic SETs. First of all, the phase of the Coulomb oscillation is shifted by the sidewall depletion gate voltage $(V_{\rm sg})$, which is useful from the point of view of SET logic. Secondly, the peak-to-valley current ratio (PVCR) decreases as the $V_{\rm cg}$ increases, due to the parasitic MOSFET effect [9]; i.e., the poly-Si control gate accumulates electrons in the Si layer under the gate, and controls the electrostatic potential of the SET island (the area of $W_{\rm ch} \times S_{\rm sg}$). This is reasonable in that a MOSFET is inevitably formed in a Si nanowire, which is also the case in various SETs with a physically formed Si island [9], [10]. Thirdly, the level of the SET current increases as the control gate voltage

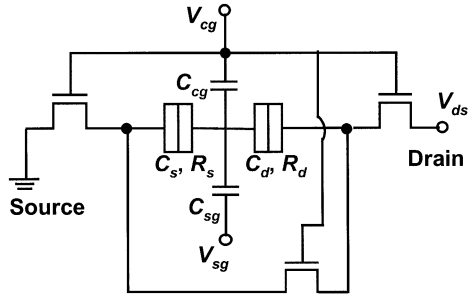


Fig. 3. Equivalent circuit model for the fabricated Si SETs with sidewall depletion gates.

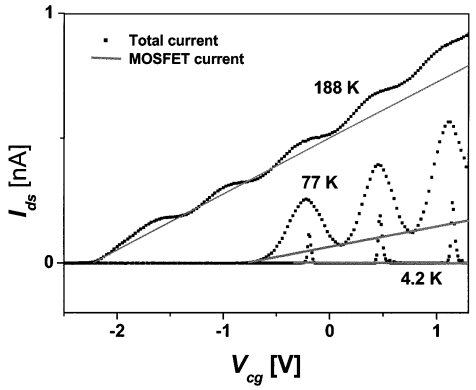


Fig. 4. Transfer characteristics of the fabricated SETs as a function of temperature. The device with an island size $S_{\rm sg} = 40$ nm is measured at $V_{\rm ds} = 5$ mV and $V_{\rm sg} = -0.1$ V.

$(V_{\rm cg})$ increases, as a result of the tunnel barrier height modulation by the $V_{\rm cg}$.

Fig. 3 shows the equivalent circuit diagram of the fabricated device, which is composed of an SET and three parasitic MOSFET's from Fig. 1, i.e., one MOSFET is parallel connected to the SET and the other two are series connected to the SET. While the two serial parasitic MOSFETs have the long channel length ($L = 3.5$ μm) and narrow width ($W_{\rm ch} = 30$ nm) from source (or drain) to island in Fig. 1, the parallel MOSFET have short channel length [L = island size + 2 × (sidewall depletion gate width)] and narrow width ($W_{\rm ch} = 30$ nm). The parallel MOSFET is not an entity physically separate from the SET, but represents the MOSFET-like current component in the SET structure due to higher energy electrons at higher temperature. In case of the SET, it has two tunnel junctions and additional capacitors. R_d and R_s are the tunneling resistances of the respective tunnel junctions. The charge of an electrically formed Si island is capacitively coupled with four capacitors, which are the control gate capacitance $(C_{\rm cg})$, the source tunnel junction capacitance (C_s), the drain tunnel junction capacitance (C_d), and the sidewall depletion gate capacitance $(C_{\rm sg})$. The back gate capacitance is assumed to be negligible due to a relatively thicker buried oxide rather than the control gate oxide.

III. Implementation of the Current–Voltage Model

In addition to the SET current $(I_{\rm SET})$, parasitic MOSFET currents inherently exist in our device. Fig. 4 shows typical experimental I–V characteristics at various temperatures. When

the control gate voltage is lower than the threshold voltage of two series-connected parasitic MOSFETs, they act as a high resistance, causing the Coulomb oscillation to vanish. As the control gate voltage increases above the threshold voltage, however, their resistance becomes low, so that we can ignore their existence. Hence, the total current (symbols) can be approximately decomposed into two components: the Coulomb oscillation of the SET and parallel-connected MOSFET current (solid lines).

The SPICE model for the realistic SETs was implemented in two parts. The total drain current is given by

$$I_{\rm ds} \cong I_{\rm SET} + I_{\rm MOSFET} \tag{1}$$

where $I_{\rm SET}$ and $I_{\rm MOSFET}$ are the SET current based on a simple capacitive Coulomb blockade model (i.e., *orthodox theory*) and a parasitic MOSFET current, respectively.

A. SET Current ($I_{\rm SET}$)

The basic formulation for the SET current is based on the analytical model proposed by Uchida *et al.* [6]. The analytical equation for the I–V characteristics of the SET having N or $N+1$ electrons in its island is given by

$$I_{\rm SET} = \frac{e}{2R_\Sigma C_\Sigma} \frac{\left(\tilde{V}_{\rm cg}^2 - \tilde{V}_{\rm ds}^2\right)\sinh\left(\tilde{V}_{\rm ds}/\tilde{T}\right)}{\left[\tilde{V}_{\rm cg}\sinh\left(\tilde{V}_{\rm cg}/\tilde{T}\right) - \tilde{V}_{\rm ds}\sinh\left(\tilde{V}_{\rm ds}/\tilde{T}\right)\right]} \tag{2}$$

where $\tilde{V}_{\rm ds} = C_\Sigma V_{\rm ds}/e$, $\tilde{T} = 2k_B T C_\Sigma/e^2$, $R_\Sigma = R_s + R_d$, $C_\Sigma = C_{\rm cg} + C_s + C_d + C_{\rm sg}$, and

$$\tilde{V}_{\rm cg} = \frac{2C_{\rm cg}V_{\rm cg}}{e} - \frac{(C_{\rm sg} + C_{\rm cg} + C_s - C_d)V_{\rm ds}}{e} - 1 - 2N. \tag{3}$$

Despite its simplicity, this analytical model perfectly reproduces the numerically calculated characteristics even in the case of a relatively high drain voltage and temperature [6]. While this result is encouraging, two important issues still remain. These are the physical effects in the real SETs, and being able to achieve a simpler form so as to incorporate the analytical equation into a conventional circuit simulator. To resolve this problem, the periodic function $\tilde{V}_{\rm cg}$ in (1) was expressed in a simplified form as follows:

$$\tilde{V}_{\rm cg} = 2\left[\frac{C_{\rm cg}}{e}(V_{\rm cg} - \Delta V) - {\rm int}\left(\frac{C_{\rm cg}}{e}(V_{\rm cg} - \Delta V) + 0.5\right)\right] \tag{4}$$

where "$\rm int(x)$" returns the largest integer $\leq x$ and the phase shift ΔV is given by

$$\Delta V = \frac{e}{2C_{\rm cg}} + \frac{(C_{\rm sg} + C_{\rm cg} + C_s - C_d)V_{\rm ds}}{2C_{\rm cg}}. \tag{5}$$

As shown in Fig. 5, (4) takes on the periodic function of $V_{\rm cg}$ with the period of $e/C_{\rm cg}$ and the phase shift of ΔV, and it is identical to one in (3). Eventually, implementing (2) and (4) into the conventional SPICE simulator is straightforward, as the circuit elements are composed of voltage-controlled current sources and voltage-controlled voltage sources.

The phase shift in Coulomb oscillation by the $V_{\rm sg}$ can be implemented by modifying ΔV. The relationship between $V_{\rm sg}$ and

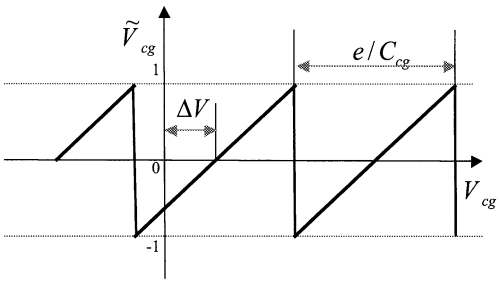


Fig. 5. Normalized $\tilde{V}_{\rm gs}$ of (4) is plotted as a function of $V_{\rm cg}$ ranging from -1 to 1.

$V_{\rm cg}$ can be derived by the following equation based on the conservation of island charge:

$$\Delta V_{\rm cg} = -\frac{2C_{\rm sg}}{C_{\rm cg}}\Delta V_{\rm sg}. \tag{6}$$

Adding the right term of (6) to (5), the final phase shift ΔV of the Coulomb oscillation is given by

$$\Delta V = \frac{e}{2C_{\rm cg}} + \frac{(C_{\rm sg} + C_{\rm cg} + C_s - C_d)V_{\rm ds}}{2C_{\rm cg}} - \frac{2C_{\rm sg}}{C_{\rm cg}}V_{\rm sg}. \tag{7}$$

In addition, the SET current increases as the $V_{\rm cg}$ increases, since the electrically induced tunnel barrier by the $V_{\rm sg}$ is lowered [8], as shown in Fig. 2. Such *tunnel barrier lowering* effect is simply included by substituting the total resistances of the tunnel junctions of (2) with (8)

$$R_\Sigma = R_\Sigma \exp[({\rm TBL}(V_{\rm cg} - V_{\rm th})] \tag{8}$$

where $V_{\rm th}$ is the threshold voltage of the parasitic MOSFETs, which are described in the next section, and TBL is a fitting parameter.

B. Parasitic MOSFET Current ($I_{\rm MOSFET}$)

The basic formulation of the parasitic MOSFET is based on the SPICE LEVEL 3 MOSFET model, where the drain current model includes the temperature dependence of both the threshold voltage and the mobility. The model was modified as shown in (9)–(11)

$$I_{\rm MOSFET} = {\rm CAL}\frac{\mu(T)\cdot W_{\rm ch}\cdot C_{\rm OX}}{S_{\rm sg} + 2W_{\rm sg}} \cdot [(V_{\rm cg} - V_{\rm th})V_{\rm ds}]\cdot f(T) \tag{9}$$

$$\mu(T) = U0\cdot(T/300)^{\rm BEX} \tag{10}$$

$$V_{\rm th} = {\rm VT0} + {\rm DT}\cdot k_b T/q \tag{11}$$

where $C_{\rm OX}$ is the control gate oxide capacitance, $W_{\rm sg}$ is the width of the sidewall depletion gate, VT0 is the zero temperature threshold voltage, $U0$ is the mobility at 300 K, and both BEX and CAL are fitting parameters. The second term in (11) is used to account for the temperature dependence of the threshold voltage, as shown in Fig. 4, including the fitting parameter DT.

Besides the threshold voltage change versus temperature, it was observed that, as the temperature increases from 4.2 K to 188 K, the slope of the current increases, which contrasts with the temperature dependence of the mobility in a conventional

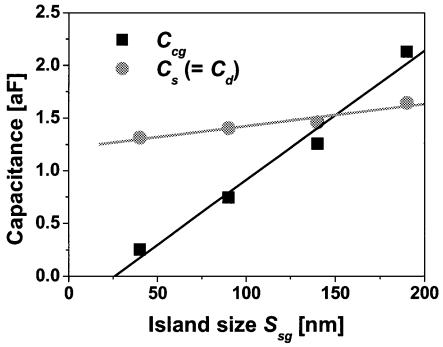
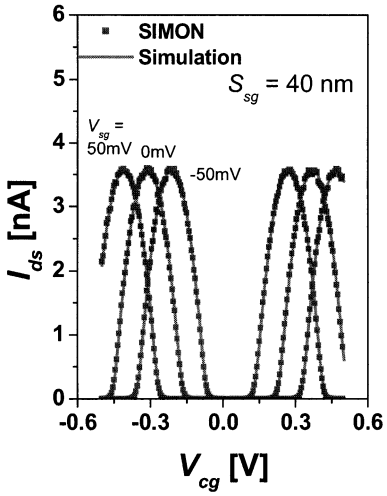
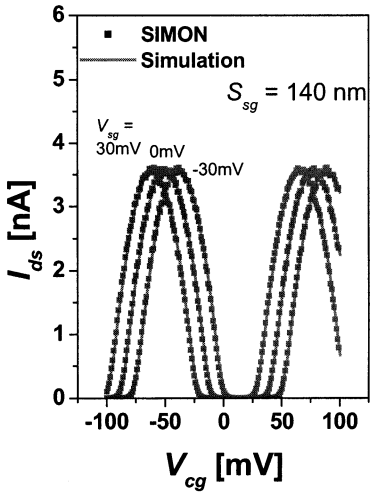


Fig. 6. Island size dependence of the device parameters. The linear regression lines agree well with the measured data obtained from 21 dies. Here, ALPHA and BETA are 1.2×10^{-17} and 2.1×10^{-18}, respectively.



(a)



(b)

Fig. 7. SET I–V characteristics using the SET SPICE model and the simulator, SIMON, for various $V_{\rm sg}$ at 4.2 K. $V_{\rm ds} = 20$ mV and $R_s = R_d = 1.4$ MΩ. (a) $C_s = C_d = 1.3$ aF, $C_{\rm cg} = 0.24$ aF (corresponding to $S_{\rm sg} = 40$ nm), and $V_{\rm sg}$ ranges from −50 to 50 mV. (b) $C_s = C_d = 1.46$, $C_{\rm cg} = 1.26$ aF (corresponding to $S_{\rm sg} = 140$ nm), and $V_{\rm sg} =$ ranges from −30 to 30 mV.

Si MOSFET. In order to understand this unusual behavior, the thermally activated conduction through the two tunnel barriers electrically induced by the $V_{\rm sg}$ should be considered. The

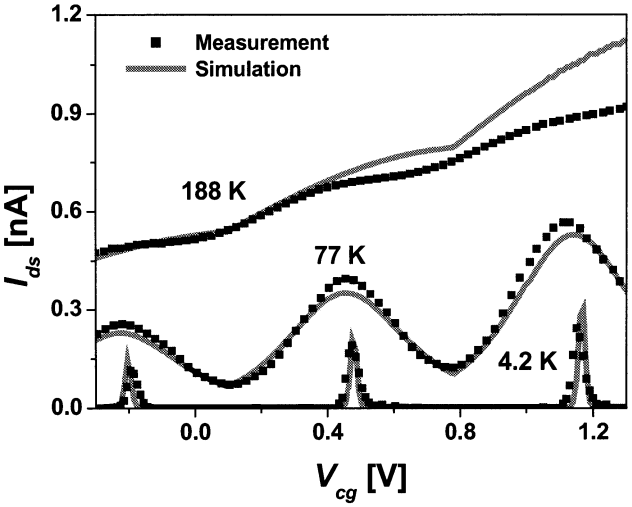


Fig. 8. SET I–V characteristics of the SETs at various temperatures ($V_{\rm ds} = 1$ mV, $V_{\rm sg} = -1$ V). Here, $C_{\rm cg} = 0.24$ aF and $C_s = C_d = 1.3$ aF (corresponding to $S_{\rm sg} = 40$ nm).

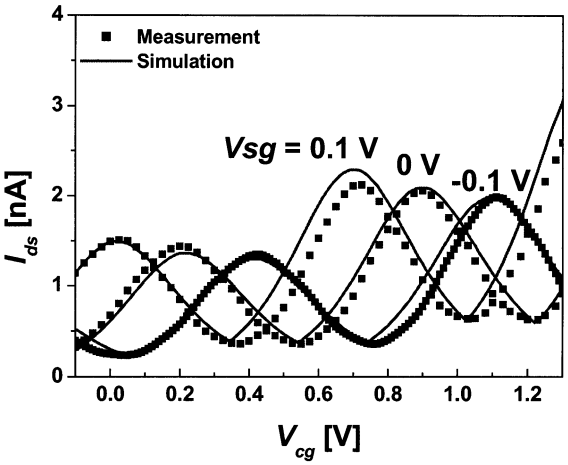


Fig. 9. SET I–V characteristics of at various sidewall gate biases at 77 K ($V_{\rm ds} = 5$ mV). Here, $C_{\rm cg} = 0.24$ aF and $C_s = C_d = 1.3$ aF (corresponding to $S_{\rm sg} = 40$ nm).

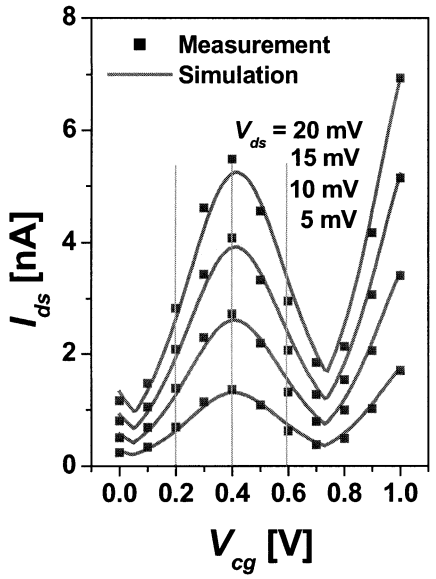
electrical behavior of the parasitic MOSFET can be modeled as thermionic emission transport, as is the case in a Schottky barrier diode [11], where the current density is given by the concentration of electrons with energies sufficient to overcome the potential barrier by the sidewall depletion gates. Thus, the thermionic emission current term $f(T)$ in (9) is given by

$$f(T) = \mathrm{RA} \cdot T^2 \exp\left(-\frac{q\Phi_B}{kT}\right) \tag{12}$$

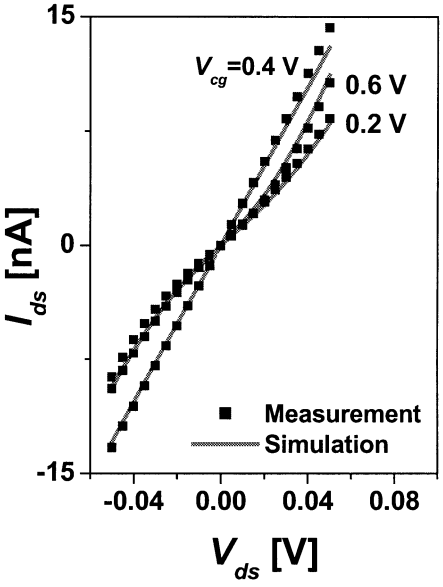
where Φ_B is the barrier height of the tunnel junctions and RA is the normalized Richardson constant.

C. Island Size Dependence of I–V Characteristics

The SPICE model for the island size dependence of the device characteristics in the fabricated SETs was implemented in two parts. For the parasitic MOSFETs, the parameter, $S_{\rm sg}$, for island size is considered in (9). On the other hand, in our previous work [9], it was found that both $C_{\rm cg}$ and C_d extracted from the SET characteristics can be represented as a linear function of



(a)



(b)

Fig. 10. I–V characteristics of the SET at various $V_{\rm ds}$ at 77 K. Here, $S_{\rm sg} = 40$ nm, $C_s = C_d = 1.3$ aF, $C_{\rm cg} = 0.24$ aF. (a) $V_{\rm cg}$–$I_{\rm ds}$ curves and (b) $V_{\rm ds}$–$I_{\rm ds}$ curves.

the island size, $S_{\rm sg}$, as illustrated in Fig. 6. The island size can be implemented into our model using the following equations:

$$C_{\rm cg} = \text{ALPHA}\,\frac{S_{\rm sg}\cdot W_{\rm ch}}{T_{\rm ctrl}} \tag{13}$$

$$C_d(=C_s) = \text{BETA}\,\frac{W_{\rm ch}}{W_{\rm sg}}\,S_{\rm sg} \tag{14}$$

where $T_{\rm ctrl}$ is the thickness of the control gate oxide, and both ALPHA and BETA are fitting parameters.

IV. Comparison With Experimental Results

In order to validate our model, the I–V characteristics at 4.2 K (at this temperature, a parasitic MOSFET is fully turned off) calculated by our SPICE model were first compared with

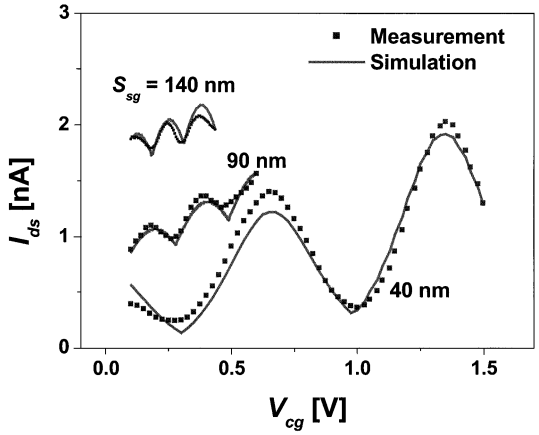


Fig. 11. I–V characteristics of the SET at various island sizes $S_{\rm sg}$ at 77 K ($V_{\rm ds} = 10$ mV, 77 K).

TABLE I
Model Parameters for the Fabricated SETs and Their Typical Values Used in the Calculations

Name	Unit	Meaning	*Value*
S_{sg}	nm	Island size	40, 90, 140
W_{sg}	nm	Width of the sidewall depletion gate	30
W_{ch}	um	Width of SOI wire	0.03
R_s (R_d)	MΩ	Tunnel resistance	1.40
C_s (C_d)	aF	Drain (Source) capacitance	1.30, 1.40, 1.46
C_{cg}	aF	Control gate capacitance	0.24, 0.76, 1.26
C_{sg}	aF	Sidewall gate capacitance	0.23
C_{ox}	F/cm²	Gate oxide capacitance in MOSFET	1×10^{-9}
U0	Cm²/Vsec	Mobility at 300 K	1500
RA	A/K²	Normalized Richardson constant	1.44×10^{-11}
Φ_B	eV	Tunnel barrier height	0.016
VT0	V	Threshold voltage at 0 K	0.23
BEX	NONE	Mobility parameter for temperature	-1.95
DT	NONE	Fitting parameter	-100
CAL	NONE	Fitting parameter	2.3×10^{-9}

those obtained from the Monte Carlo simulation, as shown in Fig. 7. The symbols represent the results calculated by the single-electron circuit simulator SIMON [2]. The simulation results from the SPICE model reproduce the Coulomb oscillation phase shift accurately in the case of two SETs with the different island sizes. This means that by using the simplification used in our model, the analytical SET model can be reasonably incorporated into the SPICE model.

The simulation result from our SPICE model was then compared with the experimental data from the fabricated SETs. First, the temperature dependence of the Coulomb oscillation from our SPICE model was compared with the measured I–V characteristics of the SETs, as shown in Fig. 8. Here, it should be emphasized that the two valley currents agree very well with each other, because the parasitic MOSFET effect is accurately reproduced in our SPICE model. Furthermore, the line shape of the Coulomb oscillation peak and its temperature dependence also agree with each other. This suggests that the assumption of both the tunnel barrier lowering and the thermionic emission current is quite reasonable and was successfully implemented

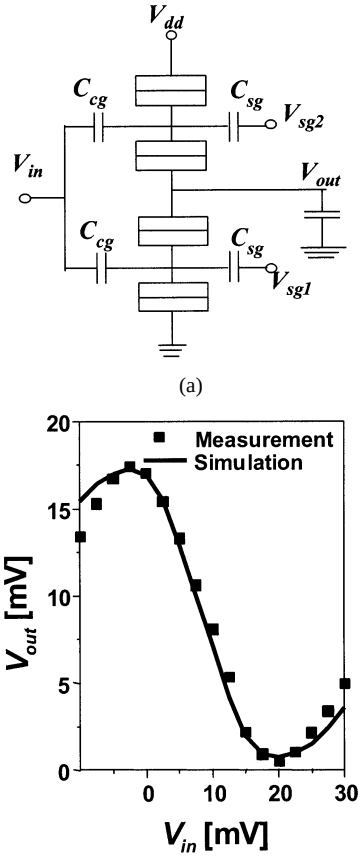


Fig. 12. (a) Circuit diagram for a complementary SET inverter consisting of two SETs in series and (b) simulated voltage transfer characteristics. Here, $V_{dd} = 20$ mV, $C_s = C_d = 1.6$ aF, and $C_{\rm cg} = 2.1$ aF, and the load capacitance $C_L = 500$ pF.

into our SPICE model. Secondly, the $V_{\rm sg}$ dependence of the Coulomb oscillation from our SPICE model was compared with the measured I–V characteristics of the SETs, as shown in Fig. 9. The Coulomb oscillation phase shift by $V_{\rm sg}$ was well reproduced, and in good agreement with the measured data. Thirdly, the $V_{\rm ds}$ dependence of the I–V characteristics from our SPICE model was compared with the measured I–V characteristics of the SETs, as shown in Fig. 10.

Furthermore, the I–V characteristic dependence on the island size was simulated, as shown in Fig. 11. The model parameter values used are shown in Table I. In particular, only one set of parameters is needed to simulate the I–V characteristics. Our model provides a good accuracy for an island size of $S_{\rm sg} = 40$ nm, 90 nm, and 140 nm at 77 K.

Finally, based on our model, a SPICE simulation was performed for a complementary SET inverter, as shown in Fig. 12. The accuracy of the voltage transfer characteristics of an SET inverter obtained from the SPICE simulation was within 15% of the measured data.

V. Conclusion

A practical SPICE model for real Si SETs was developed based on a simple analytical model and its appropriate modification. This new SPICE model can reproduce not only the typical Coulomb oscillation of the SETs but also the effects of real SETs such as the oscillation phase shift by $V_{\rm sg}$ and the parasitic MOSFET effect. This SPICE model will be very useful for estimating the realistic performance of CMOS/ SET hybrid circuits or SET logic circuits.

References

[1] M. Kirihara, N. Kuwamura, K. Taniguchi, and C. Hamaguchi, "Monte Carlo study of single-electron devices," in *Abstracts Int. Conf. Solid State Devices and Materials*, Yokohama, Japan, 1994, pp. 328–330.

[2] C. Wasshuber, H. Ksoina, and S. Selberherr, "SIMON—A simulator for single-electron tunnel devices and circuits," *IEEE Trans. Computer-Aided Design*, vol. 16, pp. 937–944, Sept. 1997.

[3] M. Fujishima, S. Amakawa, and K. Hoh, "Circuit simulators aiming at single-electron integration," *Jpn. J. Appl. Phys.*, vol. 37, pp. 1478–1482, 1998.

[4] M. Kirihara, K. Nakazato, and M. Wagner, "Hybrid circuit simulator including a model for single electron tunneling devices," *Jpn. J. Appl. Phys.*, vol. 38, pp. 2028–2032, 1999.

[5] Y. S. Yun, S. W. Hwang, and D. Ahn, "Macromodeling of single-electron transistors for efficient circuit simulation," *IEEE Trans. Electron Devices*, vol. 46, pp. 1667–1671, Aug. 1999.

[6] K. Uchida, K. Matsuzawa, J. Koga, R. Ohba, S. Takagi, and A. Toriumi, "Analytical single-electron transistor (SET) model for design and analysis of realistic SET circuits," *Jpn. J. Appl. Phys.*, vol. 39, pp. 2321–2324, 2000.

[7] D. H. Kim, S. K. Sung, K. R. Kim, B. H. Choi, S. W. Hwang, D. Ahn, J. D. Lee, and B. G. Park, "Si single-electron transistors with sidewall depletion gates and their application to dynamic single-electron transistor logic," in *IEDM Tech. Dig.*, 2001, pp. 151–154.

[8] D. H. Kim, S.-K. Sung, K. R. Kim, J. D. Lee, B.-G. Park, B. H. Choi, S. W. Hwang, and D. Ahn, "Silicon single-electron transistors with sidewall depletion gates and their application to dynamic single-electron transistor logic," *IEEE Trans. Electron Devices*, vol. 49, pp. 627–635, Apr. 2002.

[9] A. Fujiwara, Y. Takahashi, H. Namatsu, K. Kurihara, and K. Murase, "Suppression of effects of parasitic metal–oxide–semiconductor field-effect transistors on Si single-electron transistors," *Jpn. J. Appl. Phys.*, vol. 37, pp. 3257–3263, 1998.

[10] H. Ishikuro and T. Hiramoto, "Fabrication of nano-scale point contact metal–oxide–semiconductor field-effect-transistors using micrometer-scale design rule," *Jpn. J. Appl. Phys.*, vol. 38, pp. 396–398, 1999.

[11] H. Fukui, M. Fujishima, and K. Hoh, "Single-electron transistor in silicon-on-insulator with Schottky-contact tunnel barriers," *Jpn. J. Appl. Phys.*, vol. 36, pp. 4147–4150, 1997.

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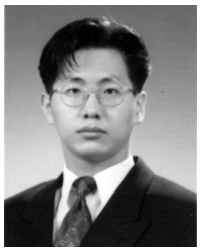

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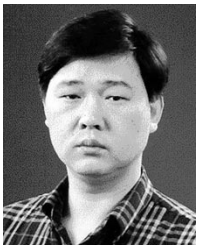

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