Si Single-Electron Transistors with Sidewall Depletion Gates and their Application to Dynamic Single-Electron Transistor Logic

Dae Hwan Kim, Suk-Kang Sung, Kyung Rok Kim, Bum Ho Choi*, Sung Woo Hwang*, Doyeol Ahn*, Jong Duk Lee, and Byung-Gook Park

Inter-University Semiconductor Research Center (*ISRC*) and School of Electrical Engineering
Seoul National University, Kwanak-gu, Seoul 151-742, KOREA, e-mail: drlife7@snu.ac.kr
*Institute of Quantum Information Processing and Systems (*iQUIPS*), University of Seoul,
Dongdaemun-gu, Seoul 130-743, KOREA

Abstract

Si single-electron transistors with sidewall depletion gates on a silicon-on-insulator nanowire are proposed and fabricated, using the combination of the conventional lithography and process technology. The size dependence of device characteristics shows good controllability and reproducibility, and a dynamic multi-functional SET logic is successfully demonstrated at 10 K, for the first time.

Introduction

Single-electron transistors (SETs) have recently attracted much attention as a candidate for ultra-high density, low power nanoelectronic devices. To optimize the device parameters for the single-electron circuit and evaluate the usefulness of the combination between SETs and CMOSFETs [1-2], it is strongly required that SETs with the dimension beyond the limit of state-of-the-art lithography should be fabricated by the conventional VLSI technology. Moreover, the controllability and reproducibility of the fabrication method is another major issue, considering that most SETs operating at a high temperature have depended on somewhat contingent phenomena such as unintentionally introduced impurities, the disorder in quantum wires, channel depletion in constricted part, e-beam irregularity or randomly distributed nanocrystals [3-5].

In this paper, novel SETs with sidewall depletion gates on a silicon-on-insulator (SOI) nanowire are proposed and fabricated, using the combination of the conventional lithography and process technology. Clear Coulomb oscillation originated from two electrically induced tunnel junctions and the single Si island between them is observed at temperatures higher than 77 K. The size dependence of the device characteristics shows the good controllability and reproducibility, and the basic operation of dynamic multi-functional SET logic circuit is successfully demonstrated at 10 K, for the first time.

Device Fabrication and Characteristics

Fig.1 shows a schematic diagram and the cross section of the fabricated device. Electron channel in a p-type 45-nm-thick SOI nanowire is formed by the back gate bias (V_{BS}),

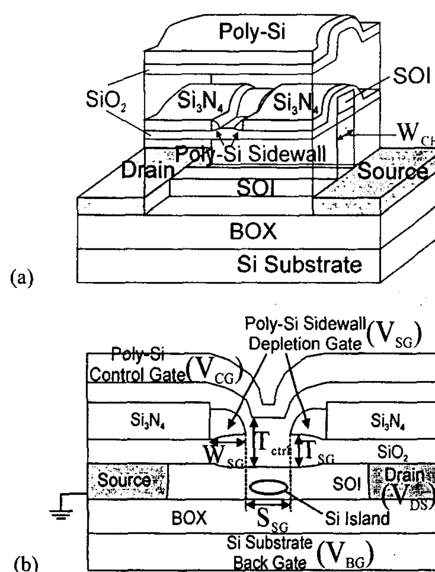


Fig. 1. (a) Schematic diagram of Si SET with sidewall depletion gates. The device was fabricated on a 45-nm-thick SOI layer. (b) Cross section of the fabricated SET. Geometrical parameters are: W_{CH}= 30 nm, T_{ctrl}= 60 nm, W_{SG}= 30 nm, T_{SG}= 38 nm. S_{SG} is varied in the range of 40-190 nm, which controls the size of Si island.

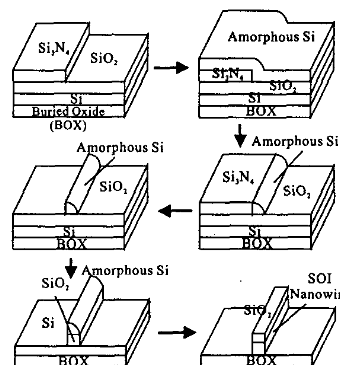


Fig. 2. Process sequence of the sidewall patterning method. The amorphous Si sidewall serves as an etch mask for the formation of an SOI nanowire.

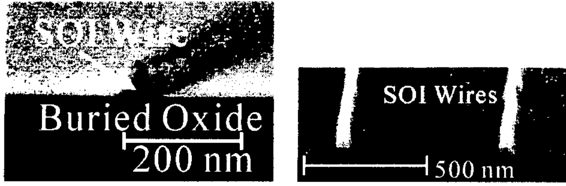


Fig. 3. SEM images of 30-nm-wide SOI nanowire. The uniformity of SOI wire formed by the sidewall patterning method efficiently prohibits the formation of unintentional tunnel junctions.

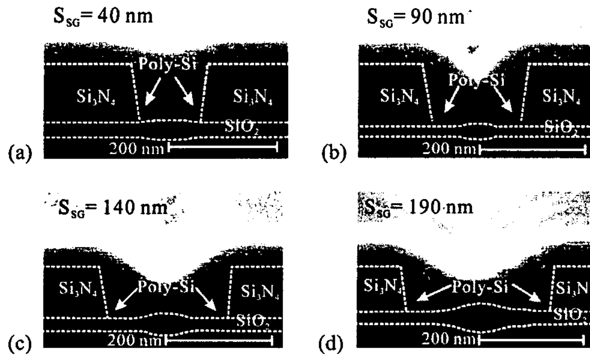


Fig. 4. SEM images of poly-Si sidewall depletion gates. The space between two sidewall gates (S_{SG}) is 40 nm (a), 90 nm (b), 140 nm (c), and 190 nm (d), respectively.

and two tunnel junctions are formed by the sidewall depletion gate bias (V_{SG}). The charge of electrostatically defined island is controlled by the control gate bias (V_{CG}).

Schematic of SOI nanowire formation technology, namely *sidewall patterning method* [6], is shown in Fig. 2. This method enables a nano-scale patterning, using the combination of the conventional lithography and process technology. Fig. 3 shows the SEM images of the uniform 30-nm-wide SOI wire formed by this method, which effectively suppressed the formation of unintentional potential barriers during the gate oxidation.

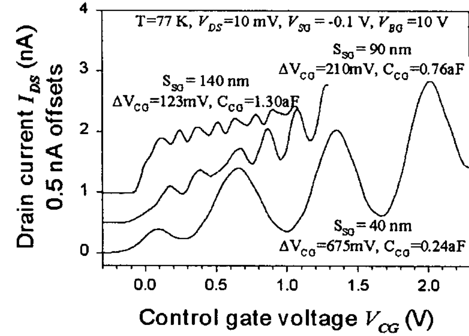
Fig. 4 shows the SEM images of polycrystalline silicon (poly-Si) sidewall depletion gates on an SOI wire. Sidewall gate structure has the merit in that it can implement a feature size smaller than the limit of e-beam lithography and depends not on the lithographical limit but on the controllability of the CVD and the plasma etching process [7]. Design parameters can be estimated from the following simple formulae

$$C_{CG} = \varepsilon_{SiO2} \times W_{CH} \times S_{SG} \times \alpha / T_{ctrl} \quad (1)$$

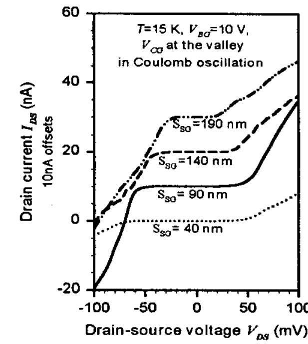
$$C_D = \varepsilon_{Si} \times X_{depl} \times W_{CH} \times \beta / W_{SG} \quad (2)$$

$$K_V = C_{CG} / C_D = 0.33 \times S_{SG} \times W_{SG} / (T_{ctrl} \times X_{depl}) \quad (3)$$

where C_{CG} is the capacitance between the control gate and island, C_S and C_D are source/drain tunnel junction capacitances, K_V is the voltage gain of SETs, ε is the dielectric constant, X_{depl} is the depletion layer depth, α is a size shrinkage factor of the electrostatically defined island, and β is a size shrinkage factor of the tunnel junction. (Other parameters are marked in Fig. 1.)



(a)



(b)

Fig. 5. The island size dependence of the I_{DS}-V_{CG} characteristics (a), and the I_{DS}-V_{DS} characteristics (b). The curves are vertically shifted by 0.5 nA (a) and 10 nA (b), respectively, for clarity.

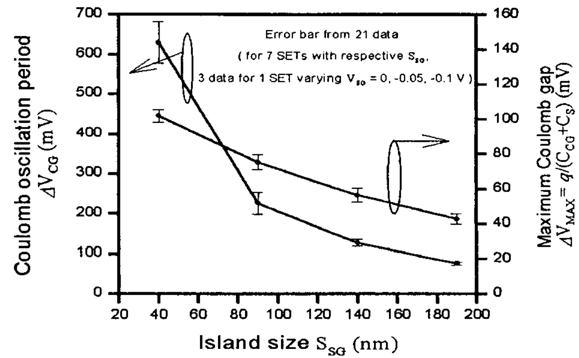


Fig. 6. The island size dependence of the Coulomb oscillation period (ΔV_{CG}) and the maximum Coulomb gap (ΔV_{MAX}). C_{CG}'s evaluated from ΔV_{CG} is 40~60 percents of the values extracted from the device geometry. The error bar shows the standard deviation for the twenty-one data taken from the seven different SETs.

Fig. 5 shows the electrical characteristics of the fabricated SETs. The size dependence of the device characteristics is clearly observed at both 77 and 15 K. The Coulomb

oscillation period (ΔV_{CG}) is 80, 123, 210, and 675 mV (C_{CG} corresponding to 2.0, 1.3, 0.76, and 0.24 aF), respectively, and the maximum Coulomb gap (ΔV_{MAX}) is 45, 59, 76, and 104 mV, respectively (Fig. 6), as S_{SG} is varied from 190 nm to 40 nm. Comparing with the device geometry, the shrinkage factor α is from 0.63 to 0.38, as S_{SG} is varied from 190 nm to 40 nm. Thus, the size of the island is effectively shrunk to 40~60 % of the defined size, due to the electric field effect.

Fig. 7 (a) shows that the critical device parameters in (1)~(3) can be reproduced and controlled by the conventional Si VLSI technologies such as CVD and RIE. As shown in the drain current contour in Fig. 7 (b), the total capacitance of the island (C_T) is from 2.86 to 5.08 aF and the voltage gain (K_V) is from 0.185 to 1.3, as the island size or the capacitive coupling between the gate and the island is increased. Moreover, ΔV_{CG} is constant as V_{CG} increases, as shown in

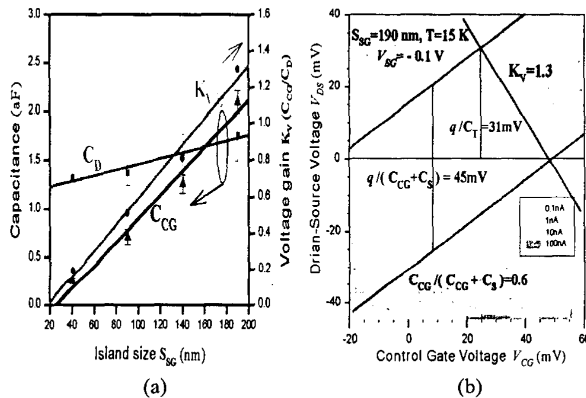


Fig. 7. (a) The island size dependence of the gate capacitance (C_{CG}), the tunnel junction capacitance (C_D), and the voltage gain (K_V). The lines by the linear regression agree very well with the form of (1)~(3). (b) The drain current contour plot of SET with 190 nm of S_{SG} at 15 K. C_T and K_V are 5.08 aF and 1.3, from the Coulomb diamond.

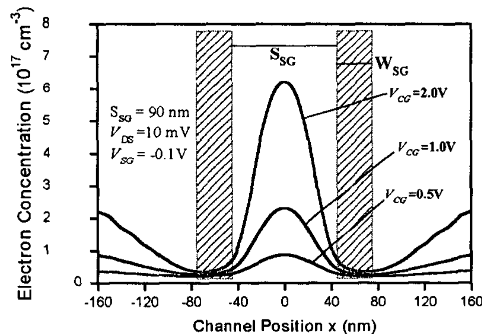


Fig. 8. Electron concentration along the SOI wire length direction. The geometry parameters for simulation are: S_{SG}=90 nm, W_{SG}=30 nm, T_{OX}=60 nm, T_{SG}=38 nm, L_{CH}= 2 μm. The size of Si island is seldom influenced, when V_{CG} increases. The potential of the island is independently controlled by V_{CG}.

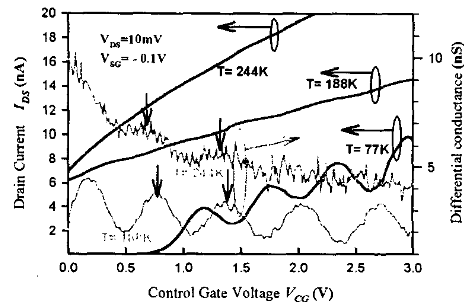


Fig. 9. The Coulomb oscillation of SET with 40 nm of S_{SG}, at temperatures above 77 K. The conductance oscillation is observed even up to 244 K as marked by arrows. The total capacitance (C_T) of Si island is 2.86 aF, which is consistent with the operation temperature of 188 K.

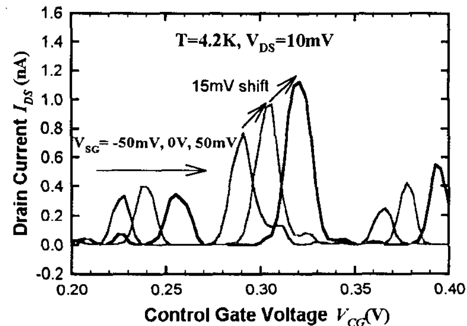


Fig. 10. Control gate voltage dependence of drain current as a function of V_{SG}. The position of Coulomb oscillation peak is modulated by V_{SG}, which is due to the sharing of island charge between the top control gate and sidewall depletion gates. Drain current level decreases as the tunneling resistance is increased by V_{SG}.

Fig. 5 (a). These characteristics stem from the strong controllability of the tunnel barriers by V_{SG}, which is attributed to three-dimensional structure of the sidewall depletion gate wrapping the SOI wire and can be confirmed by the three-dimensional device simulation as shown in Fig. 8. Considering that the characteristics of the previously reported SETs based on electrically induced island was too sensitive to gate bias conditions to maintain the reliable multiple switching performance, and that a small number of peaks was observed only in the subthreshold region [8, 9], the fabricated SETs are much improved and comparable to SETs based on the physically formed island [10].

SET with 40 nm of S_{SG} shows a clear Coulomb oscillation at 188K, and the conductance oscillation is observed even at 244K, as marked by arrows in Fig. 9. The operation temperature of 188K is consistent with 2.86 aF of C_T.

On the other hand, the position of Coulomb oscillation peak is modulated by V_{SG} as shown in Fig. 10, which is originated from the sharing of the island charge between the top control gate and sidewall depletion gates. The position of Coulomb oscillation peak controlled by the depletion gate

bias without additional gates is an advantageous feature, from the viewpoint of SET logic integration.

Dynamic Multi-functional SET Logic Circuits

The dynamic [1] four-input multi-functional SET logic gate [2] was demonstrated at 10 K, based on the peak position control of V_{SG}. Figure 11 (a) shows the equivalent circuit diagram of the dynamic multi-functional SET logic composed of one nMOSFET and two SETs. The nMOSFET switched by V_{CLK} is utilized as a pull-up device. C_L is charged up to 20 mV during the *precharge* period, and the *evaluation* is performed during the "OFF" period of nMOSFET. The V_{CG}'s of two SETs are two logic inputs, and the current switching of two SETs is determined by the states of the combinations of two V_{SG}'s, as shown in Fig. 11 (b) and (c). Figure 12 shows the experimental demonstration of the dynamic multi-functional SET logic circuit in Fig. 11 (a). Four waveforms of output voltages show the successful operations of $V_{CG1}+V_{CG2}$, $V_{CG1}\bullet V_{CG2}$, $V_{CG1}\bullet V_{CG2}$, and $V_{CG1}\bullet V_{CG2}$, respectively, for four combinations of two V_{SG}'s. Though logic levels of input and output are mismatched, the waveform of output voltage shows the full swing operation.

Conclusion

Novel SETs with sidewall depletion gates on an SOI nanowire were proposed and their application to the dynamic SET logic was successfully demonstrated at 10 K for the first time, using the combination of the conventional lithography and the process technology. The size dependence of the device characteristics showed good controllability and reproducibility. Further optimization of the device parameters will enable the design of high temperature SETs for SET logic circuit.

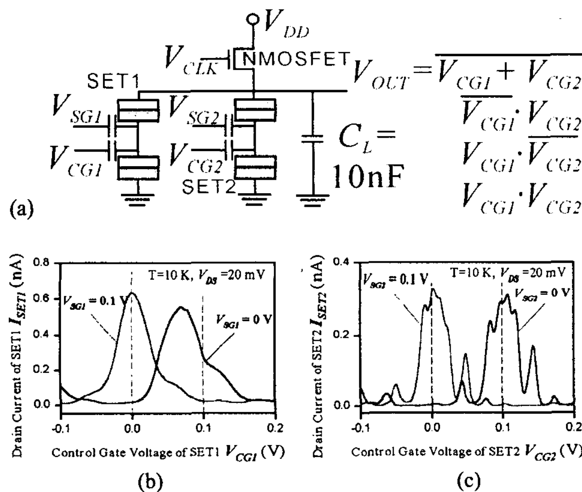


FIG. 11. (a) Equivalent circuit diagram of the dynamic multi-functional SET logic composed of one nMOSFET and two SETs. Two V_{CG}'s are two logic inputs, and the output is determined by the states of the combinations of two V_{SG}'s. (b) Peak position shift of SET1 current at 10 K. Logical "HIGH" state corresponds to 0.1 V, and "LOW" state to 0 V. (c) Peak position shift of SET2 current at 10 K.

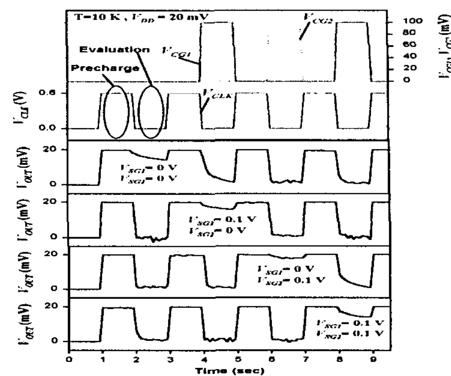


FIG. 12. Experimental demonstration of the dynamic multi-functional SET logic circuit. Four waveforms of output voltages show the successful operations of $V_{CG1}+V_{CG2}$, $V_{CG1}\bullet V_{CG2}$, $V_{CG1}\bullet V_{CG2}$, and $V_{CG1}\bullet V_{CG2}$, respectively. The supply voltage and operation temperature were 20 mV and 10 K, respectively.

Acknowledgements

This work has been supported by BK 21 program and the national program for "Tera-bit Level Nano Device Project" as a part of 21st Century Frontier Project. The work at *iQUIPS* has been supported by Creative Research Initiative (CRI) program, Korean Ministry of Science and Technology.

References

[1] K. Uchida, K. Matsuzawa, and A. Toriumi, "A new design scheme for logic circuits with single electron transistors," *Jpn. J. Appl. Phys.* vol. 38, pp. 4027-4032, 1999.

[2] K. Uchida, J. Koga, R. Ohba, and A. Toriumi, "Room-temperature operation of multifunctional single-electron transistor logic," *Tech. Dig. IEDM*, pp. 863-865, 2000.

[3] R. A. Smith and H. Ahmed, "Gate controlled Coulomb blockade effects in the conduction of a silicon quantum wire," *J. Appl. Phys.* vol. 81, pp. 2699-2703, 1997.

[4] H. Ishikuro and T. Hiramoto, "Quantum mechanical effects in the silicon quantum dot in a single-electron transistor," *Appl. Phys. Lett.* vol. 71, pp. 3691-3693, 1997.

[5] L. Zhuang, L. Guo, and S. Y. Chou, "Room temperature silicon single-electron quantum-dot transistor switch," *Tech. Dig. IEDM*, pp. 167-169, 1997.

[6] K. R. Kim, D. H. Kim, J. D. Lee, and B. G. Park, "Single-electron transistors based on silicon-on-insulator wire patterned by sidewall masking technology and electrically induced tunnel barriers," *Abstr. of Si Nanoelectronics Workshop*, pp. 42-43, 2001.

[7] U. S. Patent No. 6,211,013 (3 April 2001)

[8] D. H. Kim, D. H. Chae, J. D. Lee, and B. G. Park, "Room temperature operation of a single-electron switch with an electrically formed quantum dot," *57th DRC Dig.*, pp. 134-135, 1999.

[9] Y. Satoh, H. Okada, K. Jinushi, H. Fujikura, and H. Hasegawa, "Voltage gain in GaAs-based lateral single-electron transistors having schottky wrap gates," *Jpn. J. Appl. Phys.* vol. 38, pp. 410-414, 1999.

[10] Y. Takahashi, H. Namatsu, K. Kurihara, K. Iwadate, M. Nagase, and K. Murase, "Size dependence of the characteristics of Si single-electron transistors on SIMOX substrates," *IEEE Trans. Electron Devices*, vol. 43, pp. 1213-1217, 1996.