Demonstration of Unsupervised Learning With Spike-Timing-Dependent Plasticity Using a TFT-Type NOR Flash Memory Array

Chul-Heung Kim, Soochang Lee, Sung Yun Woo, Won-Mook Kang, Suhwan Lim, Jong-Ho Bae, Jaeha Kim, *Senior Member, IEEE*, and Jong-Ho Lee, *Fellow, IEEE*

***Abstract*— We investigate the characteristics of a synaptic imitation device using a thin-film transistor (TFT)-type NOR flash memory cell with a half-covered floating gate. The long-term potentiation (LTP) and long-term depression (LTD) required for the operation of the spike-timing-dependent plasticity (STDP) algorithm are implemented using the proposed pulse scheme. Unsupervised learning is successfully demonstrated by applying the STDP learning rule through software MATLAB simulation reflecting the LTP/LTD characteristics of the fabricated TFT-type NOR flash memory array. We present the learning and recognition processes of 28 × 28 MNIST handwritten digit patterns. First, STDP learning in a single-neuron string (784 × 1) is investigated, after which STDP learning is demonstrated in a multineuron array (784 × 10) with a lateral inhibition function to demonstrate the ability of multipattern learning and recognition. Meanwhile, we investigate the key factors of STDP unsupervised learning. Finally, an approach is suggested to implement a hardware neural network using the conventional CMOS technology for STDP unsupervised learning as a visual pattern recognition system.**

***Index Terms*— Neuromorphic, NOR flash memory, pattern recognition, spike-timing-dependent plasticity (STDP), thin-film transistor (TFT), unsupervised learning.**

I. Introduction

RECENTLY, neuromorphic systems have been studied in an effort to overcome the limitations of the von Neumann architecture [1]. Given that the existing von Neumann computer architecture is very limited in terms of speed and power consumption for high-level recognition applications and processing, research on and the development of neuromorphic technology to resolve these issues have been active areas [2]. In the field of software, research on deep neural networks (DNNs) using back-propagation algorithms [3] has been highlighted for its excellent cognitive ability, and efforts have been made to apply the findings to the hardware neural network (HNN) [4], [5]. Another aspect of implementing such an HNN is to use the spike-timing-dependent plasticity (STDP) algorithm, one of several learning algorithm that mimics the biological behavior of how the synapses operate in the brain [6]. Thus far, there have been many reports on pattern recognition systems which work via supervised learning based on a DNN [4], [7]. However, there are many applications where brain-inspired unsupervised learning can also be used in actual machine learning [8]. In order to implement an HNN using the STDP algorithm, it is important to imitate long-term potentiation (LTP)/long-term depression (LTD) functionalities as electrical elements according to the spike firing sequence in actual biological synapses and neurons [9]. Many studies have attempted to reproduce synaptic plasticity with electronic devices through the CMOS very large scale integration circuits [10], [11]. In addition, several circuits which simulate biological neurons have been reported [12]. In recent years, studies on the construction of a synapse array using a memristor crossbar array have been actively conducted [13]–[17]. However, the memristors still have disadvantages in terms of device characteristic fluctuations and reliability when constructed as a large-scale crossbar array [18], [19]. The device characteristic fluctuation of memristors causes degradation of the recognition rate in the pattern recognition process on the actual artificial neural network [20]. In order to overcome these problems, research on an electric synapse based on a CMOS field-effect transistor (FET) has been carried out recently. As a result of these efforts, several devices have been introduced, including NOMFETs [21] and MemFlash [22]. However, in one of these studies [21], metal nanoparticles are used for the memory function, causing a compatibility issue with the CMOS process. In [22], the method used to construct a large neural array and the method of operating it remain unclear. In this paper, we fabricate a thin-film transistor (TFT)-type NOR flash memory array using the conventional CMOS fabrication process and suggest an approach to use TFT-type NOR flash memory as synapse-like neuromorphic hardware. The fabricated NOR flash array structure can easily be used to form a large-scale neural network, and it is possible to update the neuron unit synapse weight through a pulse scheme, also

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The authors are with the Inter-University Semiconductor Research Center, School of Electrical and Computer Engineering, Seoul National University, Seoul 151-742, South Korea (e-mail: jhl@snu.ac.kr).

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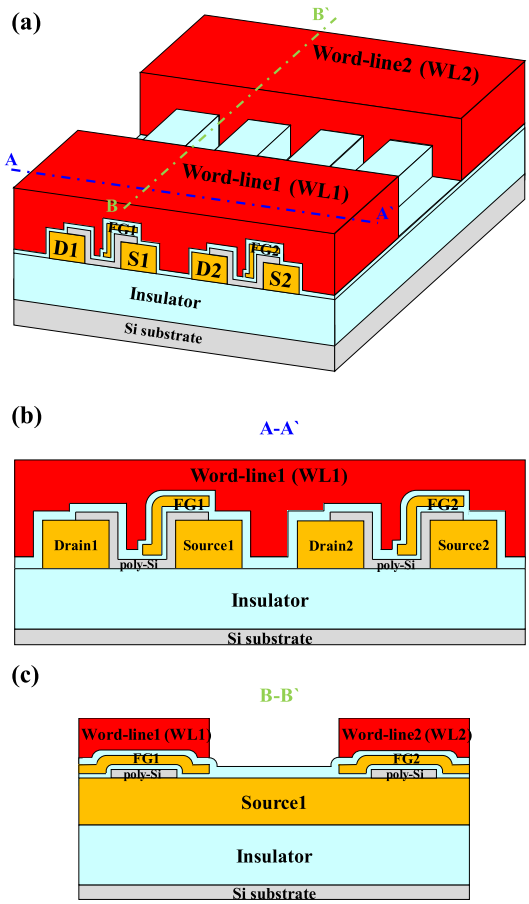

Fig. 1. (a) Bird's eye view of a TFT-type NOR flash memory array and cross-sectional views cut in the (b) WL direction and (c) BL direction.

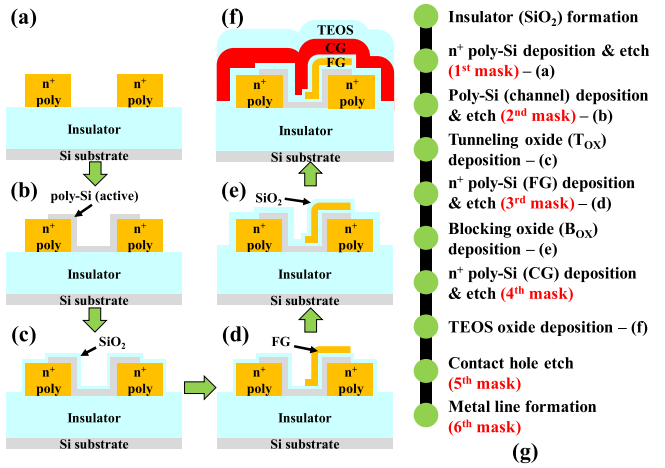

Fig. 2. (a)–(f) Schematic cross-sectional views of the key fabrication process steps. (g) Process flow of the fabrication of TFT-type NOR flash memory.

proposed here, thereby mitigating the need for an additional control circuit. Finally, we report successful simulation results of unsupervised learning using STDP in our TFT-type NOR flash memory array.

II. Device Structure and Fabrication

Fig. 1(a) shows a bird's eye view of a TFT-type NOR flash memory array. Cross sections cut along the directions of A–A′ and B–B′ are shown in Fig. 1(b) and (c), respectively. As shown in Fig. 1(a), each word-line (WL) and bitline (BL) intersect with each other in the form of a crossbar, which simplifies scaling memory arrays on a large scale. In Fig. 1(b), the drain and source of each device are connected by a poly-Si channel that is half-covered with an n^+ poly-Si floating gate (FG) through an interpoly dielectric material. Different devices are controlled simultaneously through a single WL. The half-covered FG is located between the WL and the source such that the program and erase memory operations take place when voltage is applied between these two electrodes. Because the FG covers only half of the channel, V_T does not fall below 0 in the full erase state of the device, thereby preventing leakage current during the operation of the device array. This results in a reduction of the standby power due to the excessive potentiation of synaptic elements during the unsupervised learning method. In Fig. 1(c), the device array structure in the BL direction can be confirmed. The FGs of adjacent devices are isolated from each other and are configured to perform their own memory operations. However, the positioning of the source and drain running side by side in the BL direction is common among n memory cells under n WLs, which enables current summing from n NOR flash memory cells. Thus, each memory cell can transmit its own memory information to the BL in the form of a summed current in a common BL. This configuration is similar to that of biological synapses, in which each synapse reflects its own weight information and combines it in the signal sent to the next neuron.

TFT-type NOR flash memory arrays are fabricated on a 6-in Si wafer with conventional CMOS process technology. The key fabrication process steps are shown in Fig. 2. A layer of n^+-doped poly-Si was formed on an insulator layer deposited on the wafer. After the doped poly-Si layer was patterned (first mask), a 20-nm-thick amorphous Si active layer was deposited, poly-crystalized by annealing, and then patterned (second mask). A 7-nm-thick layer of SiO_2 was then deposited as a tunneling oxide (T_{ox}) layer, after which a layer of n^+-doped poly-Si was formed and patterned as a FG (third mask). SiO_2 was then deposited at a thickness of 15 nm as a blocking oxide (B_{ox}) layer. The n^+-doped poly-Si was formed and patterned above the B_{ox} as control gate (CG) (fourth mask). After tetraethyl orthosilicate deposition, contact holes for the CGs, FGs, sources, and drains were formed (fifth mask). Subsequently, Ti/TiN/Al/TiN electrodes were formed by sputtering and were then patterned (sixth mask). Scanning electron microscope (SEM) images of a fabricated device are shown in Fig. 3. Fig. 3(a) shows an SEM image of the step corresponding to Fig. 2(b). Fig. 3(b) shows a bird's eye view of the same step. Fig. 3(c) and (d) shows SEM images of key fabrication steps corresponding to Fig. 2(d) and (f), respectively. For the fabricated cell devices in the array, the width of the CG (W_{CG}) is 2 μm and the length between the source and drain (L_{CG}) is 0.5 μm. One memory cell can be scaled down to 8 F^2 if the W_{CG} is scaled to the minimum feature size (F).

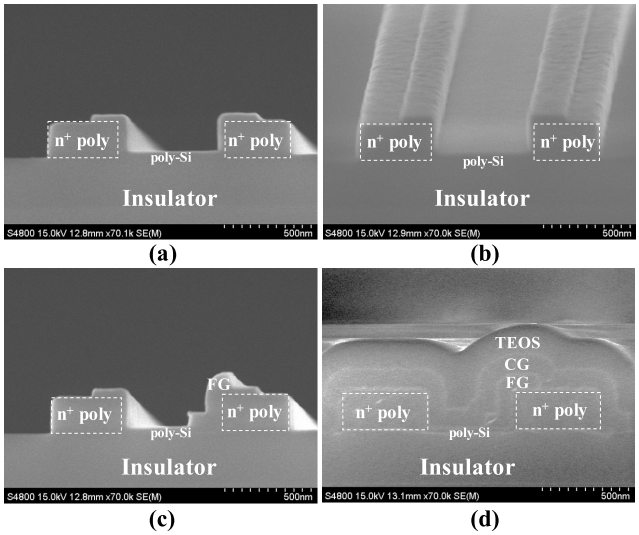

Fig. 3. SEM cross-sectional images of fabricated structures. (a) and (b) Images corresponding to the step shown in Fig. 2(b). (c) Image corresponding to the step shown in Fig. 2(d). (d) Image corresponding to the step shown in Fig. 2(f).

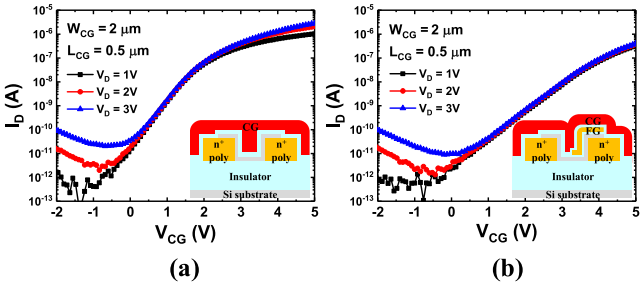

Fig. 4. Drain current versus CG bias of fabricated TFTs as a parameter of the drain voltage (V_D). (a) Reference FET (no FG). (b) TFT-type NOR flash memory cell. There is no net charge in the FG.

III. Device Measurement Results as a Synapse Device

The I_D–V_{CG} characteristics of a reference TFT and a TFT-type NOR flash memory cell as a parameter of V_D are shown in Fig. 4(a) and (b), respectively. The memory device with the FG has a larger subthreshold swing and lower ON-current value compared to the reference FET because the oxide between the CG and FG increases the effective gate oxide thickness. All of the memory cells fabricated in an array show similar I_D–V_{CG} characteristics in their initial state. The charge stored in the FG of each memory cell is reflected in the on current, which flows to the common BL in the array, having the same effect as a weighted sum in the synapse processes. Fig. 5 shows the circuit topology of a neural network system when implemented with a TFT-type NOR flash memory array. The pattern images transmitted from the PRE neurons are input into the WLs of the memory cells. The signals input to the WLs are converted into current by reflecting the weights stored in the synapses and are then summed in the common drain line (CDL) of the array. The current in the CDL flows to the POST neuron circuitry outside the array via a current mirror circuit. The current is accumulated in the membrane capacitor of the POST neuron, causing the neuron to fire if the

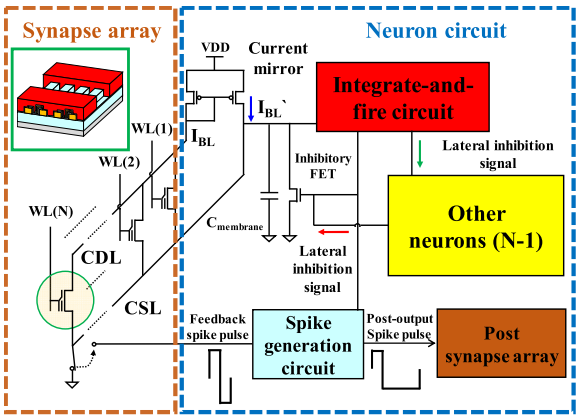

Fig. 5. Schematic circuit diagram of an unsupervised neuromorphic network with a TFT-type NOR flash memory array and a neuron circuit.

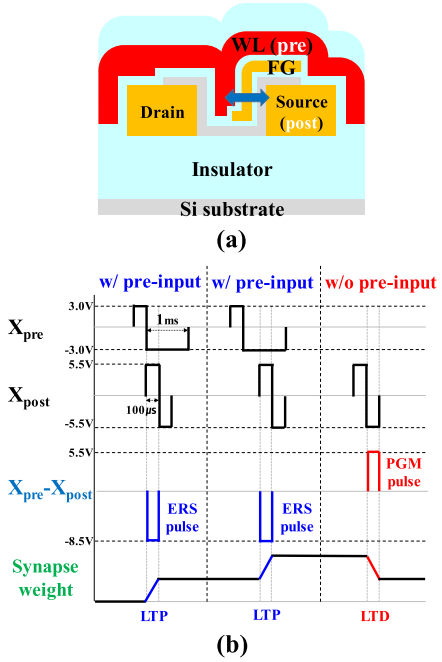

Fig. 6. (a) Schematic of PRE (input) and POST (feedback) electrodes that cause a weight update and (b) pulse scheme of PRE and POST neurons to the TFT-type NOR flash memory array that causes an LTP and LTD by erasing (ERS) and programming (PGM) of the memory cell.

membrane potential exceeds a certain threshold. Each POST neuron is connected via an FET-type inhibitory synapse that performs an inhibition action, thereby suppressing the firing actions of neurons other than itself. The firing signal of the POST neuron triggers a switch between the common source line (CSL) and the ground so that the CSL can be connected to the spike generation circuit. The firing signal is also transferred to a spike generation circuit which generates a feedback spike pulse to the CSL of its own array and an output spike pulse to the WLs of the synapse array in the next layer. In this way, neuron-based synapse weight updates can be done without additional circuitry or sequential update procedures.

For the STDP operation, the synapse cells can be potentiated or depressed selectively using the pulse scheme shown in Fig. 6. The basic principles of LTP/LTD operation in

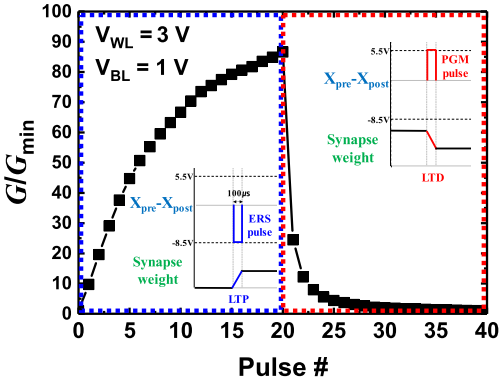

Fig. 7. LTP/LTD repetition characteristics of a device measured using the pulse scheme of Fig. 6.

TABLE I
BIAS CONDITIONS FOR THE WEIGHT-UPDATE (LTP/LTD) AND WEIGHT-READ OPERATIONS OF CELLS IN A SYNAPSE ARRAY

	LTP (w/ pre-input)	LTD (w/o pre-input)	Weight read
V_{WL}	-3 V	0 V	3 V
V_{CSL}	5.5 V	-5.5 V	0 V
V_{CDL}	floating	floating	1 V
Time	100μs	100μs	100μs

synapse cells are as follows. When a certain neuron is fired, the synapse cells that contribute to the neuron's firing are subjected to the LTP process by overlapping the input signal with the feedback signal from the neuron. On the other hand, in the case of synapse cells in which no input signal is input, the feedback signal itself is subjected to the LTD process. The pulse scheme of this type has been studied in [20]. As shown in Fig. 6(a), input signals from the PRE neurons and a feedback signal from the spike generation circuit are applied to the WLs and the CSL, respectively, to change the weights of synapse cells. The program and erase operation of the charge stored in the FG is performed according to the voltage state of the WL and the source connected to the CSL. When the input pulse is applied and the neuron is fired, the tail portion of the input pulse overlaps the head portion of the feedback pulse, as represented by the LTP operation shown in Fig. 6(b). A pulse of -8.5 V, as represented by $X_{\text{pre}} - X_{\text{post}}$ in Fig. 6(b), is then applied to the WL for 100 μs, resulting in the erase operation in the FG, which mimics the LTP operation of the synapse. In contrast, when there is no input signal from the PRE input, only the feedback pulse is applied to the source of the memory cell. This is equivalent to applying a pulse with a magnitude of 5.5 V and a width of 100 μs to the WL, which stores electrons in the FG (program operation), having the same effect as the LTD of the synapse. Table I summarizes the pulse schemes for these weight-update and weight-read operations. During the weight update, the CDL electrode is floated, which reduces power consumption by preventing leakage current that may occur during the programming and erasing of the device. A read pulse of 3 V for reading and summing the weights of the

TABLE II
FITTING PARAMETER VALUES OF MODEL EQUATIONS FOR THE SIMULATION

	LTP	LTD	
Model equation	$\delta G = e^{(a+bG+cG^2)}$	$\delta G = -(A_0 + A_1 G + A_2 G^2 + A_3 G^3 + A_4 G^4)$	
Parameter	$a = -19.56$	$A_0 = -4.263 \times 10^{-11}$	$A_3 = -2.811 \times 10^{15}$
	$b = 2.11 \times 10^{7}$	$A_1 = 0.1186$	$A_4 = 4.1064 \times 10^{22}$
	$c = -2.94 \times 10^{15}$	$A_2 = 6.7244 \times 10^{7}$	

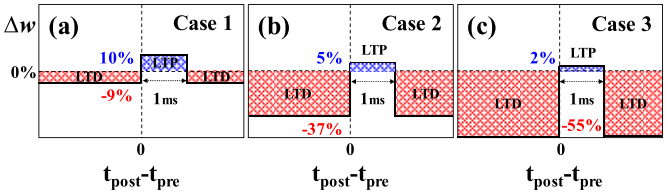

Fig. 8. STDP behavior depending on the current weight in a synaptic device when the current weight is (a) low (case 1, low G/G_{min}: 19.7), (b) moderate (case 2, moderate G/G_{min}: 56.1), and (c) high (case 3, high G/G_{min}: 79.3).

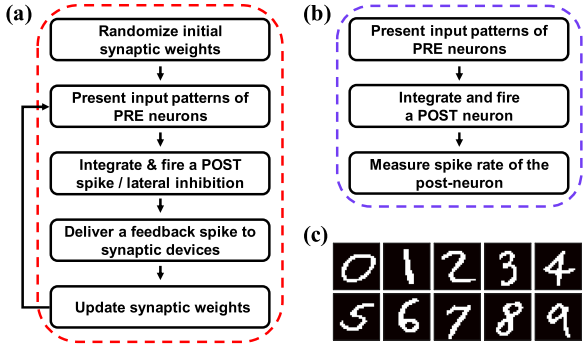

Fig. 9. Flowchart of pattern (a) learning and (b) recognition, and (c) 10 28 $\times$ 28 MNIST handwritten digits used in this simulation.

synapses is applied to the WL for 100 μs. The pulse scheme for the synapse weight update described above was applied to actual devices; these results are shown in Fig. 7. Twenty sequential repetitive LTP pulses followed by 20 repetitive LTD pulses are applied to the WL and the source electrode of the device, after which the weight of the device is read. In this case, the pulse scheme used in each operation is identical to the pulse scheme in Table I. The repeated increase of the synapse weight is confirmed by the repeated application of the LTP pulse, which is dependent on the amount of charge stored in the FG. Therefore, the degree of the weight update depends on the state of the weight of the synapse element, and it is necessary to model these characteristics to perform system-level simulation. The behavioral modeling results and the parameters used are summarized in Table II. This modeling yields individual STDP actions according to the weight state of the synapse. Fig. 8 shows the STDP curves for the three representative weight states derived from the modeling results.

IV. SIMULATION RESULTS OF PATTERN CLASSIFICATION

Fig. 9(a) and (b) shows a flowchart of the overall pattern learning and recognition processes used in the simulation, respectively. The simulation was performed with MATLAB,

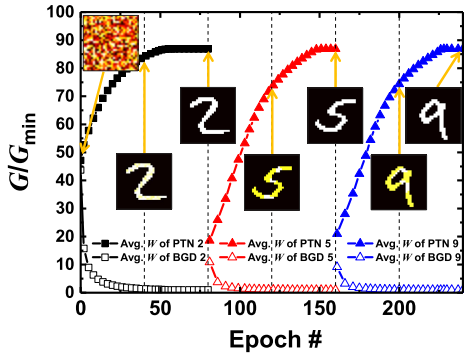

Fig. 10. Unsupervised pattern learning and updating results with a single neuron. Average weights of the targeted pattern synapses (PTN, solid symbols) and the background synapses (BGD, open symbols) when the first pattern 2, the second pattern 5, and the third pattern 9 in Fig. 9(c) were learned 80 times in order. Inset: weight map of the synapse array at the time of each epoch.

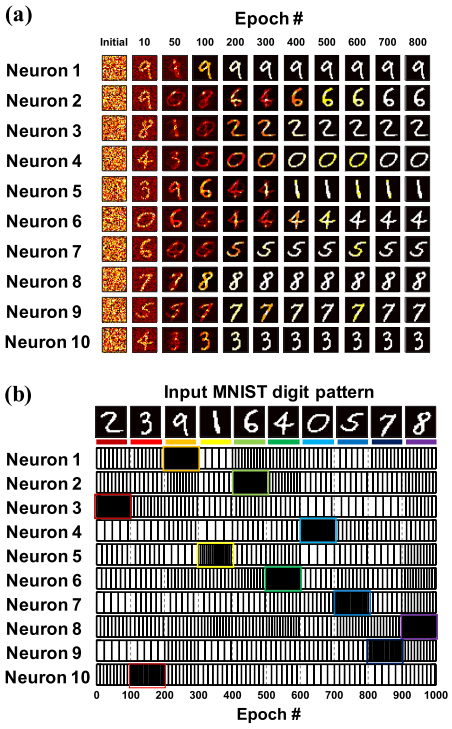

Fig. 11. Result of unsupervised multipattern learning and recognition with the multineuron array. (a) Process of changing the weights of the synapses corresponding to each neuron is shown when patterns 0–9 in Fig. 9(c) were randomly presented 800 times. (b) Classification behavior of neurons when random digit patterns are applied after the multipattern learning process.

and the operating characteristics of a synapse were determined by the measured characteristics of a TFT-type NOR flash memory cell. It was assumed that a neuron consists of an ideal capacitor and a comparator. The pattern learning process is illustrated in Fig. 9(a). First, we randomize the weights of all synapses to initialize the synaptic array. In the PRE target images for learning, only the parts where the input value of the pixels exist in the corresponding images, trigger to input X_{pre} pulse in Fig. 6(b) to the WLs of the pixels, which can cause the firing of the POST neuron through the integrate-and-fire circuit. This POST synaptic spike is transmitted to other neurons and inhibits them by discharging the accumulated charges in the integrate capacitors of the neurons. This process allows each neuron to learn its own unique image pattern, thus implementing pattern classification. The fired neuron also transmits its feedback spike to the CSLs of the synapse cells connected to it, which immediately updates the synapse weights. Fig. 9(b) explains the recognition process in neurons connected to learned synapses. Note that additional circuitry such as that for lateral inhibition and feedback spike transfers is not required during the recognition process. When target image is input, the resulting POST neuron spike through the integrate-and-fire circuit can be observed. At this time, the recognition result can be confirmed by comparing the firing rate of the learned neuron with the firing rates of other neurons. Fig. 9(c) shows the 10 28 $\times$ 28 MNIST handwritten target digits used in this learning simulation.

Fig. 10 shows the pattern learning process in a single neuron containing 784 (28 $\times$ 28) synaptic devices (i.e., 784 $\times$ 1). It is confirmed that the synaptic weights of the array update correctly based on the STDP action in the synapse array when each image is presented 80 times sequentially. The inset figures show the weight of each synapse in the array when each input pattern is applied. The initial synaptic weights are randomly distributed between the minimum to maximum weights of the proposed memory cells. The weight learning for pattern 2 is completed through 80 epochs, and after 80 consecutive epochs, learning of the weights corresponding to pattern 5 has been achieved, and after 80 succeeding epochs, weight learning for pattern 9 has been completed. This result shows that the learning of the desired input pattern and pattern updating are performed successfully. For the proposed unsupervised pattern learning, there are no additional input signals (such as the input noise used in [15]) which consume more power and make the learning process more complex. In this single-neuron learning process, the range of synaptic weights has an important influence on the pattern recognition rate. There should be a certain level of weight difference between targeted synapses and background synapses to distinguish the desired pattern from unlabeled patterns in the pattern recognition process. Therefore, it is highly desirable to maximize the range of synapse weights by optimizing the memory characteristics and pulse scheme of the device for more accurate pattern classification.

Fig. 11 shows the pattern learning and recognition results for a multineuron array (784 $\times$ 10) composed of 784 PRE-input neurons and 10 POST neurons. To implement the lateral inhibition function, inhibitory synapses are used to lower the membrane potential of neurons other than the fired neuron. This inhibitory synapse is realized by an inhibitory FET connected to the membrane capacitor of each neuron, as shown in Fig. 5. As shown in Fig. 5, each POST neuron is connected to each other through this inhibitory FET. An inhibitory factor (in this case 47%), which determines the amount of membrane potential reduction in neurons except fired neuron, should be considered carefully. If the inhibitory factor is too high, only a small number of neurons will fire repeatedly, interfering with the learning of other neurons, while if it is

too low, it will be difficult to distinguish each neuron's own learning pattern. Fig. 11(a) shows the progress of multineuron learning when the input digit patterns are presented repeatedly through the PRE input of the synaptic array. This shows the process of changing the weight states of the synapses corresponding to each neuron at representative epoch numbers. In the early stages of learning, there are oscillations of the pattern weights, but after a certain number of epochs, the weights of the synapses belonging to each neuron are gradually tuned according to a different pattern. The classification ability of patterns using the synapse array that has undergone this multipattern learning process is shown in Fig. 11(b). Fig. 11(b) shows how POST neurons fire in response to each input pattern when 10 digit patterns are applied in a random order. The digit pattern can be recognized by comparing the POST firing rate of a neuron that learned the digit pattern with the POST firing rate of other neurons. Thus, 10 distinct patterns in a multineuron array can be effectively distinguished.

V. Conclusion

Here, we fabricated successfully a TFT-type NOR flash memory to be used in a synapse array for unsupervised learning using the STDP learning algorithm. The fabrication process of the TFT-type NOR flash memory device was explained and its characteristics as an electronic synapse device were analyzed. Because the structure can perform program/erase operations by changing the gate and source voltages, it is possible to implement the STDP characteristic of a synapse without any additional circuit configuration. In addition, WLs and BLs are configured as the crossbar types, enabling excellent scalability for large-scale synapse arrays. Moreover, unsupervised learning with the STDP learning rule was demonstrated in a TFT-type NOR flash memory array. Through MATLAB simulation, the learning of 28 $\times$ 28 MNIST handwritten digit patterns was done based on the STDP characteristics of the NOR flash devices, and the pattern recognition performance was investigated. It was confirmed that learning and recognition are possible in single- (784 $\times$ 1) and multineuron (784 $\times$ 10) arrays. We presented the feasibility of implementing a scalable pattern recognition neuromorphic system using our NOR flash memory devices through system-level software MATLAB simulation.

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Chul-Heung Kim received the B.S. degree in electrical engineering from Seoul National University (SNU), Seoul, South Korea, in 2013, where he is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering.

He is with the Inter-University Semiconductor Research Center, SNU. His current research interests include neuromorphic systems and its application in computing.

Soochang Lee received the B.S. degree in electrical engineering from Seoul National University, Seoul, South Korea, in 2016, where he is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering.

His current research interests include neuromorphic systems and its application in computing.

Sung Yun Woo received the B.S. degree in electrical engineering from Kyungpook National University, Daegu, South Korea, in 2014. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Seoul National University (SNU), Seoul, South Korea.

He is currently with the Inter-University Semiconductor Research Center, SNU. His current research interests include neuromorphic systems and neural networks.

Won-Mook Kang received the B.S. degree in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2014. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Seoul National University, Seoul.

His current research interests include neuromorphic systems.

Suhwan Lim received the B.S. and M.S. degrees in electrical engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2008 and 2010, respectively. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Seoul National University, Seoul, South Korea.

His current research interests include neuromorphic systems and neural networks.

Jong-Ho Bae received the B.S. degree in electrical engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2011. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Seoul National University (SNU), Seoul, South Korea.

He is currently with the Inter-University Semiconductor Research Center, SNU.

Jaeha Kim (SM'09) received the B.S. degree in electrical engineering from Seoul National University, Seoul, South Korea, in 1997, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1999 and 2003, respectively.

He is currently an Associate Professor with Seoul National University. His current research interests include low-power mixed-signal systems and their design methodologies.

Jong-Ho Lee (F'16) received the Ph.D. degree in electronic engineering from Seoul National University (SNU), Seoul, South Korea, in 1993.

He was a Post-Doctoral Fellow with the Massachusetts Institute of Technology, Cambridge, MA, USA, from 1998 to 1999. He has been a Professor with the School of Electrical and Computer Engineering, SNU, since 2009.