Comparative Study on Program/Erase Speed, Retention, and Process Margin for Manufacturability of High Performance Metal Nanocrystal Memories

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Abstract

A comparative study on P/E speed, retention, and the process margin of various metal nanocrystal (NC) memories including high-*k* and bandgap engineering technologies is performed by using TCAD simulation. It is shown that NC memory with the bandgap engineered bottom oxide is superior in terms of all of program/erase speed, retention, and process margin. Furthermore, the merit of a high-*k* top oxide becomes prominent only in the case of the diameter of NC smaller than 4 nm.

I. Introduction

Recently, memory structures employing discrete trap as the charge storage media have been under the active research and development as the promising candidates to replace DRAM or Flash memories. Whereas the exact characterization and engineering of nitride trap parameters (*i.e.*, spatial distribution, energy level, and program/erase (P/E) cycling effects) have been emerged as very challenging issues in the cases of nitride-based charge trap memory technologies (*e.g.* SONOS, NROM, SANOS, and TANOS), metal nanocrystal (NC) charge trap memories have advantages in terms of superior designability (due to very controllable state-of-the-art process forming NC arrays) and better retention resulting from higher electron barrier (due to applying a high work function metal NC). Especially, high-*k* and bandgap engineering technologies have been very recently employed to metal NC memories as performance-boosters [1-3]. However, their unified guides including P/E speed, retention, and the immunity to process variations has been rarely reported in spite of previous systematic works [4-7].

In this work, the TCAD (Synopsys ISE Sentaurus) [8-9]-based comparative study on P/E speed, retention, and the process margin of various metal (cobalt) NC memory structures including high-*k* and bandgap engineering technologies are reported. In addition, the effects of NC diameter (*D*), density (*N*), and NC-to-NC space (*S*) on the memory characteristics are systematically discussed.

II. Simulation Results and Discussions

***A. Simulation Structure*:** Fig. 1 illustrates the schematic views of various metal NC memories (sample A~D). A *p*-type doping level of silicon substrate is 1×10^{17} [cm^{-3}]. Cobalt (work function ϕ_m=4.7 eV) NCs were used as charge storage media. The range of *D* and *N* is 2~7 nm and 1~2×10^{11} cm^{-2}, respectively. Table I summarizes the major simulation parameters.

***B. NC diameter effect*:** Fig. 2 shows the P/E speed of NC memories with *D*=3 nm and *S*=11 nm ($N=5\times10^{11}$ cm^{-2}), respectively. The P/E operation is performed by biasing the control gate voltage $V_P/V_E=\pm12$ V during the time T_P/T_E=30 ms, respectively, keeping the source and drain to be grounded. The sample D with Al_2O_3 (ε_r= 8.9) top oxide shows a faster P/E speed than that of the samples with SiO_2 top oxide due to enhanced bottom oxide field. Fig. 3 indicates that the *D*-dependence of ΔV_T (V_T is defined V_{GS} at I_{ds}=0.1 μA for V_{DS}=0.05 V) for all samples. The program efficiency increases with increasing *D* due to higher coupling ratio (*CR*) as seen in Fig. 3. Table II shows ΔV_T of all samples with the same injected charge (-6.6×10^{-19} C/NC) in NC. The sample A shows the largest ΔV_T at the same NC charge, and that means best efficiency translating from NC charge to the channel potential. Nevertheless, the P/E operation of sample D is faster than that of sample A due to a high-*k* effect (enhanced bottom oxide field) as shown in Fig. 2. Especially, it is worthwhile to note that the P/E efficiency of sample D becomes the worst compared with the other samples with the increase of *D*. In order to explain this complicated NC memory structure-dependence of the relation between P/E speed and *D*, Fig. 4 shows the electrostatic potential contour of the sample A and D. Under a fixed NC density *N*, the increase of *D* means the increase of both *CR* and NC spherical curvature-induced E-field enhancement as shown in Fig. 4(a). However, it is compensated in the sample D due to a high-*k* induced release of E-field as seen in Fig. 4(b). Consequently, the P/E efficiency of sample D becomes less sensitive to *D*, and the merit of higher P/E speed of sample D is diluted at *D*>4 nm. Next, in perspective of retention, Fig. 5 (a) shows the charge loss per dot for sample A. The simulation parameters are as follows: *D*=5 nm, *S*=9 nm ($N=5\times10^{11}$ cm^{-2}), V_G=0 V, and *T*=85 °C. The retention time is defined by the 10 % charge loss at the same initial charge (-8.0×10^{-18} C/NC) for all samples. As shown in Fig. 5(b), sample B with bandgap engineered bottom oxide shows better retention characteristic than those of the others. The *D*-dependence of sample D retention is less conspicuous because the increase of NC total capacitance C_{NC} (decrease of charging energy q^2/C_{NC}) with increasing *D* is relatively weak function of *D* in sample D.

***C. NC density effect*:** Fig. 6(a)~(c) show the NC density *N*-dependence of ΔV_T as a function of *D*. Fig. 6(d) shows the *N*-dependence of the number of electrons stored in a single NC. ΔV_T can be described as (1) :

$$\Delta V_T = \frac{qNp}{\varepsilon_{tun}}[t_{con} + \frac{\varepsilon_{tun}}{2\varepsilon_{nc}} D], \qquad (1)$$

where t_{con} and *p* are the thickness of top oxide and the number of electrons stored in a single NC [4]. Then, it is explainable that ΔV_T increases and is saturated or decrease again with increasing *N* under the same *D* as seen in Fig. 6(a)~(c). It is because that *p* is reduced with the increase of *N* under the same *D* as seen in Fig. 6(d). Fig. 7(a)~(c) show that the *N*-dependence of retention characteristics as a function of *D* (the same initial charge= -8.0×10^{-18} C/NC). Needless to say, the retention time decreases with the scaling of *D* due to the increase of NC charging energy. The retention time also decreases with increasing *N* due to the increase of C_{NC} with increasing *S* as shown in Fig. 8. Fig. 8(c) shows the NC conduction band minimum becomes higher by 0.4 eV due to increasing q^2/C_{NC} when *N* is changed from 2.5×10^{11} cm^{-2} to 7×10^{11} cm^{-2}.

***D. Process margin*:** Fig. 9 shows the process margin of various NC memories in perspective of *D* and *S* (eventually *N*). In each plot, five lines correspond to ΔV_T=4 V limit at $V_P/V_E=\pm12$ V during T_P/T_E=30 ms, 10 year retention limit at *T*=85 °C, NC-to-NC interaction limit (*S*=4 nm), and actual *N*/*D* limits (1×10^{11} cm^{-2}/10 nm), respectively. The area of gray region means the allowed range of *D* and *S*, *i.e.*, process margin, which is 92:104:90:101 (in the order of sample A~D). It is noticeable that sample B shows the widest process margin.

III. Conclusions

The P/E speed, retention, and the process margin of various Co NC memories including high-*k* and bandgap engineering technologies were extensively compared and benchmarked by using TCAD simulation. In addition, complicated *N* and *D*-dependence of the P/E speed and retention was systematically explained in perspective of 3D *CR*, E-field enhancement effect, high-k effect, and NC charging energy. Our results show that NC memory with the bandgap engineered bottom oxide is superior in terms of all of P/E speed, retention, and process margin. Furthermore, the merit of a high-*k* top oxide turned out to be maximized as *D* decreases. Our results give the unified insight into metal NC memory design and analysis.

Acknowledgements

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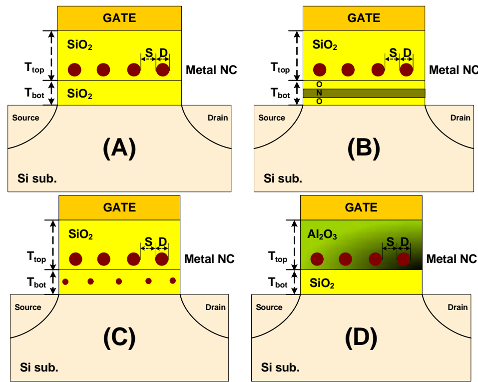

Fig. 1. The schematics of the metal NC cell. (A) Classic structure. (B) Using bandgap engineering. (C) Double layer NC. (D) Using high-K dielectric. Parameters for simulation: $T_{bot@EOT} = 3$ nm, $T_{top@EOT} = 12$ nm.

Table I. Simulation parameters of nanocrystal devices

	A	B	C	D
Bottom oxide, T_{bot}	SiO_2	O/N/O	NC / SiO_2	SiO_2
	3 nm	1.2/1/1.5	D = 1 nm / 3 nm	3 nm
Top oxide, T_{top}	SiO_2	SiO_2	SiO_2	Al_2O_3
	12 nm	12 nm	12 nm	20 nm

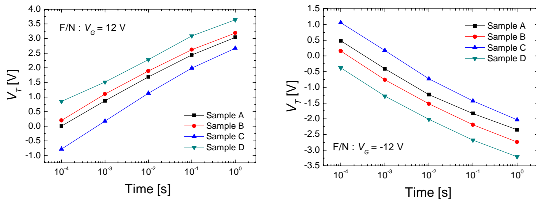

Fig. 2. The threshold voltage versus program/erase time in a metal NC memories for $D = 3$ nm, $S = 11$ nm, $N = 5 \times 10^{11}$ cm^{-2}.

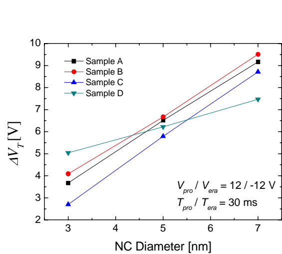

Table II. V_T for same injection charge.

V_{T1} @ same inj.Q = -6.6e-19 C				
Diameter	**A [V]**	**B [V]**	**C [V]**	**D [V]**
2 nm	**3.43**	**3.12**	**3.43**	**2.92**
3 nm	**3.17**	**2.87**	**3.16**	**2.77**
V_{T2} **@ same inj.Q = 0**				
Diameter	**A [V]**	**B [V]**	**C [V]**	**D [V]**
2 nm	**0.64**	**0.61**	**0.65**	**0.56**
3 nm	**0.61**	**0.58**	**0.62**	**0.55**
$(V_{T1}-V_{T2})/V_{T2}$	**4.36**	**4.11**	**4.28**	**4.21**
	4.20	**3.95**	**4.10**	**4.04**

Fig. 3. The ΔV_T versus NC Diameter for all samples with density $N = 5 \times 10^{11}$ cm^{-2}. P/E condition: F/N $V_P/V_E = \pm 12$ V, $T_P/T_E = 30$ ms.

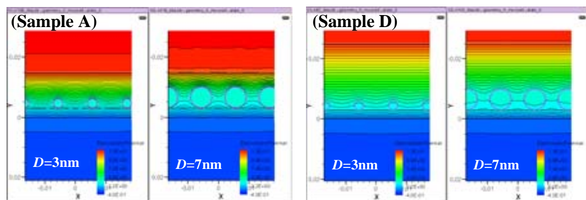

Fig. 4. Cross-sectional view of the electrostatic potential contours in the NC memory unit cell for sample A and D.

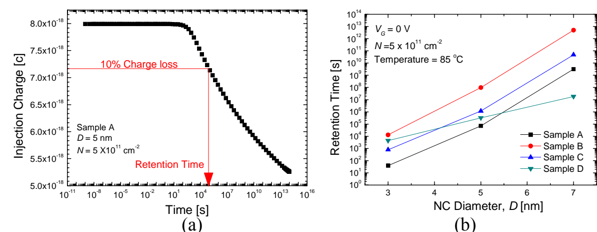

Fig. 5. Retention characteristics at $V_G = 0$ V and $T = 85$ °C. (a) Retention time is defined as the time required by the injection charge to decrease by a factor 10%. (b) Retention time versus NC diameter for respective samples.

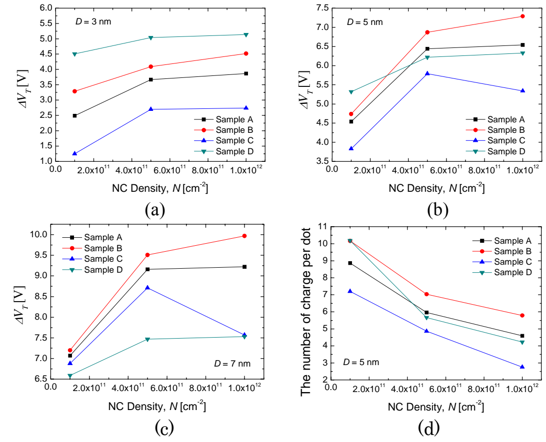

Fig. 6. (a) (b) (c). The ΔV_T versus NC density for all samples with $D = 3, 5, 7$ nm. Program/Erase condition: F/N $V_P/V_E = \pm 12$ V, $T_P/T_E = 30$ ms. (d) The number of injection charge per dot versus NC density.

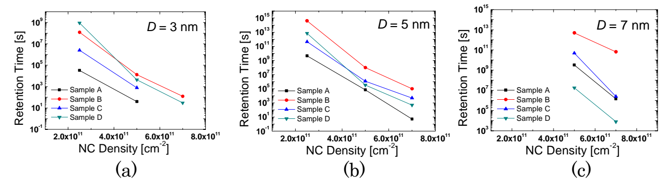

Fig. 7. (a) (b) (c) Retention time versus NC density for all samples with $D = 3, 5, 7$ nm respectively.

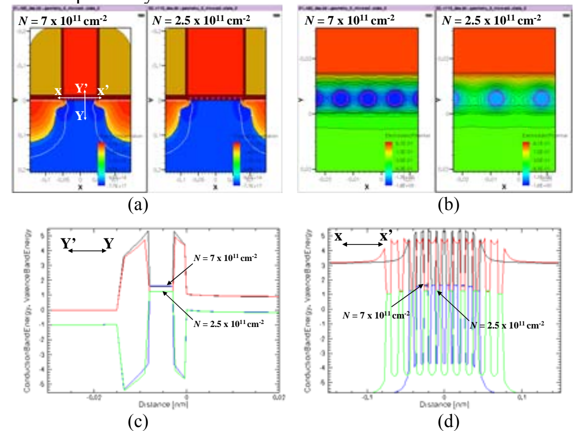

Fig. 8. (a) The schematic of the metal NC for $N = 7 \times 10^{11}$ cm^{-2} and $N = 2.5 \times 10^{11}$ cm^{-2}. (b) Cross-sectional view of the electrostatic potential contours. (c) Perpendicular band diagram. (d) Horizontal band diagram.

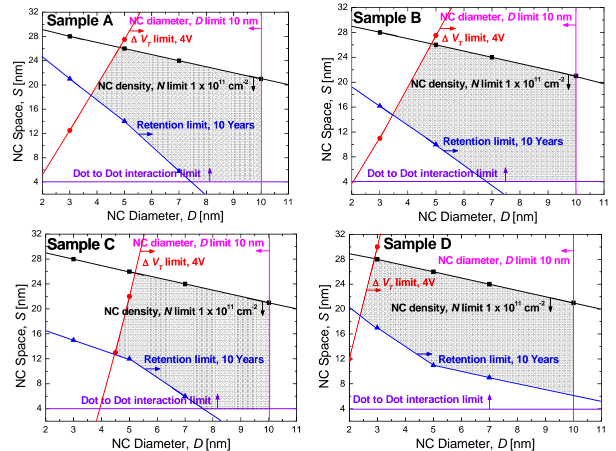

Fig. 9. Programming, erasing, and retention characteristics of NC memory design at $V_P/V_E = \pm 12$ V, $T_P/T_E = 30$ ms and $V_G = 0$ V and $T = 85$ °C. The area of gray region means the allowed range of D and S, *i.e.*, process margin, which is 92:104:90:101 (in the order of sample A~D). It is noticeable that sample B shows the widest process margin.