Modeling and Separate Extraction of Gate-Bias- and Channel-Length-Dependent Intrinsic and Extrinsic Source–Drain Resistances in MOSFETs

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***Abstract*—A new technique for a separate extraction of the current-path-dependent resistance ($R_{\rm SD0}$) from the contact-dependent source and drain resistances ($R_{\rm Se}$ and $R_{\rm De}$) is reported for a single MOSFET. We also report a technique for a separation of $V_{\rm GS}$-dependent source and drain resistance ($R_{\rm SDi}$) from the $V_{\rm GS}$- and $L_{\rm eff}$-dependent channel resistance ($R_{\rm ch}$) with multiple MOSFETs. We confirm the proposed techniques applied to n-channel MOSFETs with various W/L combinations and obtain $R_{\rm Se} = 10.5-12.4\ \Omega$, $R_{\rm De} \cong 12.7\ \Omega$, and $R_{\rm SD0} = 4.7\ \Omega$ for $W = 10\ \mu$m. $V_{\rm GS}$-dependent but L-independent $R_{\rm SDi}$ is extracted to be $2.8-4.2\ \Omega$.**

***Index Terms*—Drain resistance, extraction, extrinsic, intrinsic resistance, MOSFET, parasitic resistance, source resistance.**

I. Introduction

ACCURATE extraction of parasitic resistances caused by variations in the layout, process, and long-term device degradation is a crucial issue as MOSFETs are scaled down into deep submicrometer. Due to the electric field through the gate voltage ($V_{\rm GS}$), the intrinsic ($R_{\rm int}$) and extrinsic ($R_{\rm ext}$) parts of source (R_S) and drain (R_D) resistances are modulated by the gate bias, particularly in lightly doped drain (LDD) MOSFETs [1]–[6]. Therefore, accurate modeling and characterization of parasitic resistances in MOSFETs are required for a robust design and implementation of CMOS-based integrated circuits (ICs) and systems in CAD tools. There have been reports on extracting the parasitic series resistances in MOSFETs [7]–[13]. We also reported the parasitic junction current method (PJCM) [14] to separately extract the $V_{\rm GS}$- and effective channel length ($L_{\rm eff}$)-independent extrinsic source, drain, and substrate resistances in MOSFETs with a substrate contact.

In this letter, by combining the PJCM and the total drain-to-source resistance ($R_{\rm TOT}$) obtained from the channel resistance method (CRM) [1] under linear mode of MOSFETs, we report a new technique for a separation of the contact-dependent extrinsic resistances ($R_{\rm Se}$ and $R_{\rm De}$) from the spreading current-path-dependent extrinsic resistances ($R_{\rm S0}$ and $R_{\rm D0}$) for a single MOSFET. We also report another technique for a separate extraction of the $V_{\rm GS}$-dependent parasitic resistance ($R_{\rm Si} + R_{\rm Di}$) from the $V_{\rm GS}$-dependent channel resistance with multiple MOSFETs having different channel lengths.

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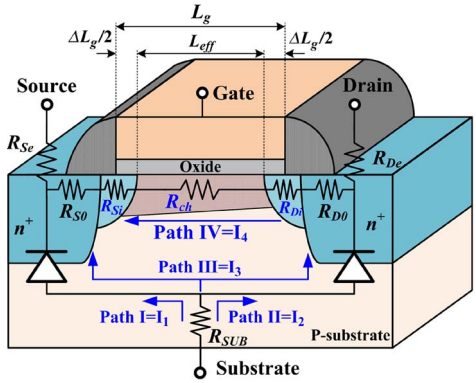

Fig. 1. Cross-sectional view and equivalent circuit for n-channel LDD MOSFETs with parasitic resistances with substrate resistance ($R_{\rm SUB}$).

II. Separate Extraction of $R_{\rm int}$ and $R_{\rm ext}$ in MOSFETs

An equivalent circuit for n-channel MOSFETs with parasitic resistances ($R_{\rm Se}, R_{\rm De}, R_{\rm SD0}, R_{\rm Si}, R_{\rm Di}, R_{\rm ch}$, and $R_{\rm SUB}$) is shown in Fig. 1. We note that $R_{\rm int} (\equiv R_{\rm S0} + R_{\rm Si} + R_{\rm ch} + R_{\rm Di} + R_{\rm D0})$ is composed of the intrinsic source and drain resistances ($R_{\rm Si}$ and $R_{\rm Di}$), which depend on $V_{\rm GS}$ but are independent of $L_{\rm eff}$, and the channel resistance $R_{\rm ch}(V_{\rm GS}, L_{\rm eff})$, which depends on $L_{\rm eff}$ as well as $V_{\rm GS}$. $R_{\rm S0}$ and $R_{\rm D0}$ are independent of $V_{\rm GS}$ and $L_{\rm eff}$ but dependent on the device structure, including the overlap and spacing S/D contact and the gate.

In the extraction of $V_{\rm GS}$- and $L_{\rm eff}$-independent *extrinsic* components ($R_{\rm Se}, R_{\rm De}$, and $R_{\rm SUB}$) in the source and drain resistances, the PJCM [14] is employed. The current under high forward bias through Path I for the substrate–source junction is limited by the series resistance $r_{\rm S1} \equiv R_{\rm Se} + R_{\rm SUB}$ while that through Path II by $r_{\rm S2} \equiv R_{\rm De} + R_{\rm SUB}$. For Path III, it is limited by $r_{\rm S3} \equiv R_{\rm SUB} + (R_{\rm Se} \| R_{\rm De})$ with $R_{\rm Se}$ and $R_{\rm De}$ in parallel. $R_{\rm SUB}$ is assumed to be constant with a symmetrical substrate contact to the source and drain in the individual MOSFET to be characterized. In the PJCM, therefore, currents through the parasitic junctions under a large forward bias are described by

$$I_i = I_{\rm Si} e^{(V_{\rm Sub} - \Delta V_i)/V_{\rm th}}, \qquad \Delta V_i = I_i \cdot r_{\rm si} \tag{1a}$$

$$r_{\rm S1} = (R_{\rm SUB} + R_{\rm Se}) \quad r_{\rm S2} = (R_{\rm SUB} + R_{\rm De})$$
$$r_{\rm S3} = (R_{\rm SUB} + R_{\rm De} \| R_{\rm Se}) \tag{1b}$$

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with $I_{\rm Si}$ as a reverse saturation current and ΔV as a voltage drop across the parasitic resistance in each configuration. We obtain extrinsic resistances

$$R_{\rm SUB} = r_{\rm S3} - \sqrt{(r_{\rm S1} - r_{\rm S3})(r_{\rm S2} - r_{\rm S3})} \quad (2a)$$

$$R_{\rm Se} = r_{\rm S1} - R_{\rm SUB} \quad R_{\rm De} = r_{\rm S2} - R_{\rm SUB} \quad (2b)$$

from the measured data by the PJCM technique.

For a separate extraction of $V_{\rm GS}$- and L-dependent *intrinsic* components $(R_{\rm int} \equiv R_{\rm S0} + R_{\rm Si} + R_{\rm ch} + R_{\rm Di} + R_{\rm D0})$, the CRM [1] is combined with the result from the PJCM. In the linear operation of MOSFETs at a low $V_{\rm DS}$ for the CRM, the drain current through Path IV is limited by the total resistance $R_{\rm TOT} (\equiv R_{\rm Se} + R_{\rm S0} + R_{\rm Si} + R_{\rm ch} + R_{\rm Di} + R_{\rm D0} + R_{\rm De})$ described by

$$I_D \cong \frac{\mu_{\rm eff} C_{\rm ox} W}{L_{\rm eff}} [((V_{\rm GS} - I_D R_S) - V_T)(V_{\rm DS} - I_D (R_S + R_D))] . \quad (3)$$

Therefore, $R_{\rm TOT}$ is obtained from experimental data via

$$\begin{aligned} R_{\rm TOT} &= (V_{\rm DS}/I_D) \\ &= (R_{\rm Se} + R_{\rm De} + R_{\rm S0} + R_{\rm D0}) + R_{\rm SDi}(V_{\rm GS}) + R_{\rm ch}(V_{\rm GS}, L_{\rm eff}) \\ &= R_{\rm ext} + \frac{\Delta L}{k_1 (V_{\rm GS} - V_T)} + \frac{L_{\rm eff}}{k_2 (V_{\rm GS} - V_T)} \end{aligned} \quad (4)$$

with $R_S \equiv R_{\rm Se} + R_{\rm S0} + R_{\rm Si}(V_{\rm GS})$ and $R_D \equiv R_{\rm De} + R_{\rm D0} + R_{\rm Di}(V_{\rm GS})$, $C_{\rm ox} = \varepsilon_{\rm ox}/t_{\rm ox}$ as the oxide capacitance per unit area, $\mu_{\rm eff}$ as the effective mobility, $L_{\rm eff}$ as the effective channel length, and $R_{\rm ch}$ as the $V_{\rm GS}$- and $L_{\rm eff}$-dependent channel resistance. We note that the source and drain resistances (R_S and R_D) are composed of $V_{\rm GS}$-independent resistance $R_{\rm ext}$ defined as

$$R_{\rm ext} \equiv R_{\rm Se} + R_{\rm S0} + R_{\rm D0} + R_{\rm De} \quad (5)$$

and $V_{\rm GS}$-dependent intrinsic resistance $R_{\rm int}$ defined as

$$R_{\rm int}(V_{\rm GS}) \equiv R_{\rm SDi}(V_{\rm GS}) + R_{\rm ch}(V_{\rm GS}, L_{\rm eff}) \quad (6)$$

with $R_{\rm SDi} \equiv R_{\rm Si} + R_{\rm Di}$. We note that $V_{\rm GS}$-independent $R_{\rm SD0}$ can be obtained from

$$R_{\rm SD0} \equiv R_{\rm S0} + R_{\rm D0} = R_{\rm TOT}|_{\rm CRM} - (R_{\rm Se} + R_{\rm De})_{\rm PJCM} \quad (7)$$

as a difference between $R_{\rm TOT}$ from the CRM at large $V_{\rm GS}$ and the $R_{\rm SDe}$ from the PJCM. This is useful in accurate modeling of MOSFETs and a robust design of CMOS-based ICs.

We also note that the channel resistance is described by $R_{\rm ch}(V_{\rm GS}, L_{\rm eff}) = L_{\rm eff} \times r_{\rm ch}$ with $r_{\rm ch}$ defined as the $V_{\rm GS}$-dependent effective channel resistance per unit length. Therefore, $R_{\rm ch}$ is proportional to $L_{\rm eff}$ while the intrinsic resistance $R_{\rm SDi}$ depends on $V_{\rm GS}$ and the structure of the device but independent of $L_{\rm eff}$. From the combination of the CRM with the PJCM for the experiment, we obtain the $V_{\rm GS}$- and $L_{\rm eff}$-dependent intrinsic resistance as

$$\begin{aligned} R_{\rm int}(V_{\rm GS}, L_{\rm eff}) &\equiv R_{\rm TOT}|_{\rm CRM} - (R_{\rm Se} + R_{\rm De} + R_{\rm S0} + R_{\rm D0})|_{\rm PJCM} \\ &= L_{\rm eff} \times r_{\rm ch}(V_{\rm GS}) + R_{\rm SDi}(V_{\rm GS}). \end{aligned} \quad (8)$$

By plotting the intrinsic resistance $R_{\rm int}(V_{\rm GS}, L_{\rm eff})$ as a function of $L_{\rm eff}$, therefore, we separate the $V_{\rm GS}$-dependent intrinsic resistance $R_{\rm SDi}(V_{\rm GS})$ from the offset and $r_{\rm ch}(V_{\rm GS})$ from the slope, respectively.

III. Experimental Results and Discussion

Experimental I_D–$V_{\rm DS}$ characteristics of an n-channel MOSFET with $t_{\rm ox} = 2.9$ nm and $W/L = 10\ \mu{\rm m}/0.3\ \mu{\rm m}$ are shown in Fig. 2(a). The threshold voltage and the subthreshold slope were measured to be $V_T = 0.21 - 0.25$ V and $SS = 77 - 80$ mV/dec, respectively. $R_{\rm TOT}$ obtained from the CRM at $V_{\rm DS} = 0.05$ V is shown in Fig. 2(b). By the PJCM for Path II (as an inset), we obtained $r_{\rm S2} = R_{\rm De} + R_{\rm SUB} = 106.7\ \Omega$ from $\Delta V_2 = I_2 \cdot (R_{\rm De} + R_{\rm SUB}) = 0.42$ V at $I_2 = 3.9$ mA. Series resistances for other two configurations are extracted to be $r_{\rm S1} = R_{\rm Se} + R_{\rm SUB} = 108.2\ \Omega$ for Path I and $r_{\rm S3} = R_{\rm SUB} + (R_{\rm Se} \| R_{\rm De}) = 100\ \Omega$ for Path III. We finally obtained $R_{\rm Se} = 12.7\ \Omega$, $R_{\rm De} = 11\ \Omega$, and $R_{\rm SUB} = 95.5\ \Omega$ through (2) for the PJCM. We confirmed that extrinsic resistances $R_{\rm Se}$, $R_{\rm De}$, and $R_{\rm SUB}$ were independent of $V_{\rm GS}$ over $V_{\rm GS} = -2.5$ to $+3.0$ V.

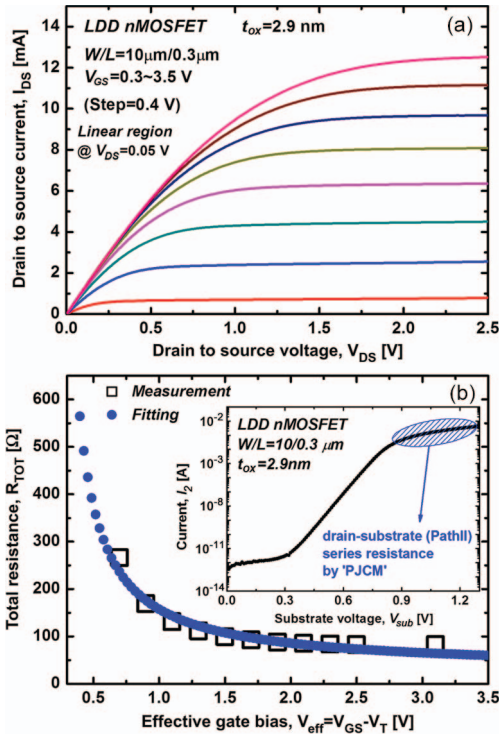

Fig. 2. (a) I_D–$V_{\rm DS}$ characteristics of the LDD n-MOSFET ($W/L = 10\ \mu{\rm m}/0.3\ \mu{\rm m}$). (b) $V_{\rm GS}$-dependent $R_{\rm TOT}$ with an inset for the voltage drop across the series resistance $r_{\rm S2} = R_{\rm De} + R_{\rm SUB}$ in the drain–substrate junction for Path II.

For a separation of the spreading path-dependent resistances ($R_{\rm S0}$ and $R_{\rm D0}$) from the contact-dependent resistances ($R_{\rm Se}$ and $R_{\rm De}$) in a single MOSFET, experimental results for an n-MOSFET with $W/L = 10\ \mu{\rm m}/0.3\ \mu{\rm m}$ are shown in Fig. 2(b) with extracted model parameters in Table I. Combining the PJCM with CRM, we obtained L-independent $R_{\rm SD0} \cong 4.68\ \Omega$ and $R_{\rm ext} = 28.38\ \Omega$ for a MOSFET with $L = 0.3\ \mu$m and $W = 10\ \mu$m. Experimental results for MOSFETs over $L = 0.13 - 0.5\ \mu$m and $W = 10\ \mu$m are summarized in Table I. A small perturbation in the result is due to process and structural variations in MOSFETs. This strongly suggests the requirement of accurate characterization through a separate extraction of resistances in each MOSFET.

For the other separate extraction of the $V_{\rm GS}$-dependent parasitic resistance $(R_{\rm Si} + R_{\rm Di})$ from the $V_{\rm GS}$-dependent channel resistance $(R_{\rm ch})$ with multiple MOSFETs having different channel lengths, extracted resistances [■ □ : $R_{\rm TOT}$; ●○ : $R_{\rm ch}(V_{\rm GS})$ and $R_{\rm SDi}(V_{\rm GS})$] are shown in Fig. 3 for a MOSFET with $W/L = 10\ \mu{\rm m}/0.3\ \mu{\rm m}$ as a function of $V_{\rm eff}$. Combining the PJCM and CRM for different channel lengths, the layout and $V_{\rm GS}$-dependent intrinsic resistances obtained from (8) are

TABLE I
EXTRACTED RESISTANCES FOR L- AND V_{GS}-INDEPENDENT R_{ext} IN n-MOSFETs WITH $W = 10\ \mu$m

L [μm]	0.13	0.22	0.3	0.5
V_T [V]	0.21	0.25	0.23	0.21
R_{De} [Ω]	12.8	12.6	12.7	12.7
R_{Se} [Ω]	11.3	10.5	11.0	12.4
R_{SD0} [Ω]	4.75	4.75	4.68	4.72
R_{ext} [Ω]	28.85	27.85	28.38	29.82

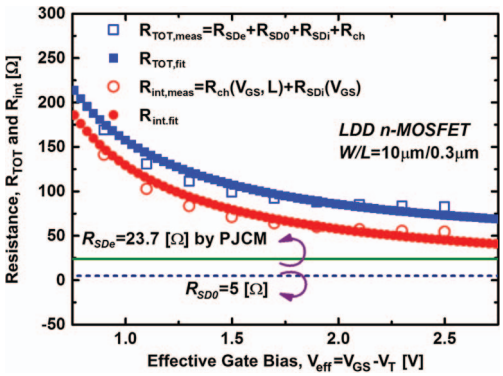

Fig. 3. $R_{\rm SDe}$, $R_{\rm SD0}$, $R_{\rm SDi}$, and $R_{\rm ch}$ obtained from a MOSFET with $W/L = 10\ \mu$m/0.3 μm.

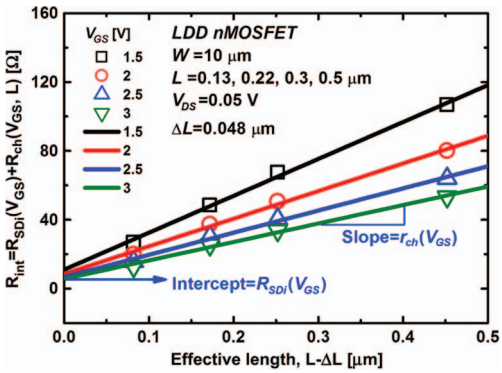

Fig. 4. $R_{\rm int}$ versus $L_{\rm eff}$ as a function of $V_{\rm eff} = V_{\rm GS} - V_T$. $r_{\rm ch}(V_{\rm GS})$ and $R_{\rm SDi}(V_{\rm GS})$ are obtained from the slope and the intercept, respectively.

TABLE II
$V_{\rm GS}$-DEPENDENT INTRINSIC RESISTANCES IN MOSFETs WITH $W = 10\ \mu$m

V_{GS} [V]	V_{GS}-dependent resistances		L=0.3 μm	L=0.13 μm
			R_{ext}=28.38 [Ω]	R_{ext}=28.81[Ω]
	R_{SDi} [Ω]	r_{ch} [Ω/μm]	R_{ch} [Ω]	R_{ch} [Ω]
1.5	4.2	205.8	51.9	16.9
2.0	3.4	154.1	38.8	12.7
2.5	3.0	122.6	30.9	10.1
3.0	2.8	101.6	25.6	8.3

shown in Fig. 4. $R_{\rm ch}(V_{\rm GS}, L_{\rm eff})$ and $R_{\rm SDi}(V_{\rm GS})$ were obtained from the slope and the intercept, respectively, in the plot of $R_{\rm int}$ versus $L_{\rm eff}$ from multiple gate lengths, and extracted intrinsic resistances are summarized in Table II for $L = 0.3$ and 0.13 μm with $W = 10\ \mu$m. We note that, with increasing gate voltage, as shown in Table II, the intrinsic resistance $R_{\rm SDi}$ gets more important in the total resistance compared with the channel resistance $R_{\rm ch}$. This also suggests that a separation of $V_{\rm GS}$-dependent $R_{\rm SDi}$ from $V_{\rm GS}$- and $L_{\rm eff}$-dependent $R_{\rm ch}$ is important in the modeling and characterization for a robust design of CMOS-based ICs.

IV. CONCLUSION

Combining the PJCM with the CRM, a new technique has been reported for a separation of the contact-dependent extrinsic resistance $(R_{\rm Se} + R_{\rm De})$ from the spreading current-path-dependent extrinsic resistance $(R_{\rm SD0})$ for a single MOSFET. We have also reported another technique for a separate extraction of the $V_{\rm GS}$-dependent parasitic resistance $(R_{\rm SDi})$ from the $V_{\rm GS}$- and $L_{\rm eff}$-dependent channel resistance $(R_{\rm ch})$ with multiple MOSFETs. In the separate extraction, the gate bias and channel length dependences of the source and drain resistances were fully considered. We applied the techniques to n-channel MOSFETs for various channel lengths $(L = 0.13{-}0.5\ \mu$m) with $W = 10\ \mu$m and $V_T \cong 0.21{-}0.25$ V. Extrinsic resistances were obtained to be $R_{\rm Se} = 10.5 \sim 12.4\ \Omega$, $R_{\rm De} \cong 12.7\ \Omega$, and $R_{\rm SD0} = 4.7\ \Omega$ for MOSFETs with $W = 10\ \mu$m. $V_{\rm GS}$-dependent but L-independent $R_{\rm DSi}$ was extracted to be $2.8{-}4.2\ \Omega$, and $R_{\rm ch}$ decreased with increasing $V_{\rm GS}$ and with decreasing channel length.

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