Density-of-States (DOS)-based I-V and C-V Models and Link to Circuit Simulator for Polymer Thin Film Transistors (PTFTs)

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Abstract

The 3 key results were reported with I-V and C-V models linked to Hspice circuit simulator for polymer-based thin film transistors (PTFTs): (1) The subgap density of states (DOS) extraction of the PTFTs by multi-frequency capacitance-voltage (MFCV) spectroscopy; (2) Analytical PTFT models based on the process-controlled parameters including subgap DOS; (3) Analytical model for circuit design incorporated into Hspice via Verilog-A. Our approach is expected to be a powerful platform for the systematic design of PTFTs.

1. Introduction

Polymer-based thin film transistors (PTFTs) are under active research for the low-cost integrated circuit and system on the flexible large-area substrate due to low temperature and printing fabrication capability [1,2]. As the demand for various applications increases, PTFT models become essential for accurate prediction of performance and systematic design of PTFT-based circuits [3]. To realize it, the density-of-states (DOS)-based models are positively necessary. We have reported that extraction of the sub-bandgap DOS ($g(E)$) in PTFT by multi-frequency capacitance-voltage (MFCV) spectroscopy [4]. Three clear motivations of this work can be summarized as (1) subgap DOS extraction of the PTFTs by MFCV spectroscopy; (2) analytical PTFT models based on the process-controlled parameters including extracted subgap DOS; (3) analytical model for circuit design and incorporation into Hspice via Verilog-A.

2. PTFT Fabrication and Device Structure

Fig. 1(a) shows an array of semitransparent polymer transistors printed on a glass substrate. Fig. 1(b) shows a schematic cross-sectional view of the PTFT with a coplanar structure. The polymer semiconductor was dissolved in tetrahydrophthalene (THN) at a concentration of 0.2 wt%, and then ink-jet printed via Dimatix printer. The fabricated PTFTs with a coplanar structure has the channel width $W=120$ μm, the gate-to-S/D overlap length $L_{Ox}=10$ μm, gate insulator thickness $T_{Ox}=300$ nm, and the thickness of polymer film $T_{Active}=50$ nm (confirmed by FIB-SEM).

3. Results and Discussion

The extraction procedure of $g(E)$ by the MFCV spectroscopy is shown in Fig. 2. Fig. 3 shows the calculation flow about numerical and analytical current-voltage (I-V) models. The models start with $g(E)$ obtained by the MFCV spectroscopy. The analytical model is based on the effective carrier density combined with a coupled-Schottky diode model for the non-linearity and the Poole-Frenkel mobility model for the lateral field-dependent carrier transport. We expect that the proposed analytical model can be employed for a fast and efficient circuit design.

Fig. 4 shows the measured and calculated $I_{DS}$-$V_{DS}$ characteristics of driver/load-PTFTs in diode-load type inverter through inkjet printing process on a glass wafer with model parameters in Table II. They agree well with each other over a wide voltage range. Fig. 5 shows the load line and VTC of the PTFT-based inverter. DC characteristics are well reproduced by the analytical model. We note that the proposed C-V model is also consistent with the measured quasi-static C-V characteristics as shown in Fig. 6(a). Calculated capacitances for the gate-to-drain ($C_{gd}$), and gate-to-source ($C_{gs}$) are shown in Fig. 6(b) as a function of the drain bias. Measured transient characteristics are compared with the Hspice simulation result based on the proposed I-V and C-V models as shown in Fig. 7.

4. Summary

In summary, we reported I-V & C-V models linked to Hspice circuit simulator for polymer TFTs with 3 key results: (1) The subgap DOS extraction of the PTFTs by MFCV spectroscopy; (2) Analytical PTFT models based on the process-controlled parameters including DOS; (3) Analytical model for circuit design incorporated into Hspice via Verilog-A. Our approach is potentially expected to be a robust platform for a systematic design of PTFTs through the material/process optimization.

Acknowledgements

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References

Fig. 1. (a) A photograph of PTFTs and circuit integrated on a glass wafer. (b) A schematic illustration of the integrated PTFT.

Fig. 2. (a) The equivalent R-C models of PTFTs (b) The calculated $C_{GS}$ from f-dependent $C_{TF}$-VGS characteristics is shown as an inset. (c) Extracted VGS-dependent $R_0$ obtained from the high frequency $|Z_{in}|$ under a fixed VGS as shown in the inset. (d) Extraction of $R_0$ using the MFCV spectroscopy.

Fig. 3. The calculation flow for the analytical I-V models with same parameters (g(E), $p_{AND}$, $N_0$). Analytical model flow: Fixed input parameters ($P_{eff}$=N_{TFD}, $kT_{eff}$=kT_{TFD}, W, L, T_{OX}, Schottky barrier ($\phi_b$)).

Table I. Extracted parameters for the driver/load PTFTs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$p_{AND}$</th>
<th>$N_0$</th>
<th>$\phi_b$</th>
<th>$V_{ON}$</th>
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<tr>
<td>Driver-TFT</td>
<td>0.146</td>
<td>2.5x10^{19}</td>
<td>0.45</td>
<td>-1.5</td>
</tr>
<tr>
<td>Load-TFT</td>
<td></td>
<td></td>
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Fig. 4. Measured $I_{DS}$-V_{GS} characteristics (symbol) of (a), the driver-PTFT and (c), the load-PTFT. The lines indicate the calculated by the extracted parameters with the analytical model.

Fig. 5. (a) Measured load line curve, (b) Measured VTC curves compared with simulated ones; they agree well with simulated ones.

Fig. 6. (a) Measured VOD-dependent $C_{GS}$-$V_{OD}$ curves, (b) Calculated $C_{GS}$-$V_{SG}$ and $C_{GD}$-$V_{SG}$ Curves by the analytical model.

Fig. 7. Measured transient characteristics (symbol) of the PTFT-based inverter circuit are compared with the proposed analytical model-based verilog-A and Hspice simulation incorporating the extracted parameters. They agree very well with each other over a wide range of $V_{SS}$.