Noise measurements: The measurements were performed using a lock-in amplifier noise measurement system with a centre frequency of 10 MHz and a noise effective bandwidth of 4.2 MHz. Pure electron (hole) injection was provided by the light of a 633 nm He-Ne laser focused to a spot onto the top p'-(n') GaAs cladding layer. Although hole initiated multiplication can be undertaken on p'-n' structures by illuminating the n' cladding layer through a hole in the substrate, this was found to cause device degradation. Consequently, the n'-p' diodes were grown to facilitate hole injection. The excess noise factor, \( F \), was determined using Bulman et al's method [5], and calculated using
\[
F = \frac{1}{2} \frac{M}{M_F},
\]
where \( M \) is the equivalent photocurrent of the silicon pin diode that produces the same noise power as the device under test (DUT). \( M_F \) is the multiplication of the DUT and \( M \) the unmultiplied primary photocurrent.

Fig. 2 Excess noise factor for pure hole injection against multiplication for GaAs n'-i-p' structures

- \( w = 0.36 \mu m \)
- \( w = 0.21 \mu m \)
- \( w = 0.10 \mu m \)
- \( w = 0.05 \mu m \)

McIntyre predictions with \( k' = 1/k \) increasing from 0 to 1 in steps of 0.1.

Figs. 1 and 2 show the excess noise factor \( F \) against multiplication for different thickness structures with electron and hole initiated multiplication, respectively. In Fig. 1 the \( w = 1.13 \mu m \) excess noise characteristics are in good agreement with those predicted by McIntyre's noise model [1] for electron initiated multiplication and published ionisation coefficients in GaAs [2]. However, with decreases in \( w \), the excess noise interpreted using McIntyre's curves reduces from that expected when \( k = \beta/\alpha = 0.55 \) for a 0.57\( \mu m \) p'-i-n', to that expected when \( k = 0.1 \) for a \( w = 0.049\mu m \) p'-i-n'. In Fig. 2, a similar reduction in \( F \) for decreasing \( w \) from \( w = 0.36\mu m \) to 0.050\mu m is shown for the hole injected n'-i-p' structures. In the 0.049\mu m p'-i-n' and 0.050\mu m n'-p' diodes, photo-multiplication values of 10 were achievable but noise measurements were limited to \( M_l = 5 \) and \( M_H = 4 \), respectively, due to the large tunneling currents saturating the noise measurement system.

At high electric fields in thin avalanche regions (\( w \leq 0.10\mu m \)), \( k \) has been shown to converge to unity to produce almost identical electron and hole photomultiplication characteristics [6]. The ionisation probabilities for electrons and holes in such thin structures are therefore very similar, contrary to the conclusion of Hu et al. An alternative hypothesis for the low noise behaviour is based on recent modelling by Herbert [7], and Ong et al. [8], who attribute the low noise in thin p'-i-n' devices to the dead space, the minimum distance a carrier must travel in the electric field to impact ionise. The dead space reduces the probability of carriers undergoing secondary ionisations, thus the distribution function for multiplication is narrower and a lower excess noise results. Since electrons and holes have similar dead spaces, this interpretation allows for a similar reduction in excess noise with hole initiated multiplication even when \( \alpha = \beta \).

Conclusion: Avalanche noise measurements on submicrometre diodes have shown there is decreasing excess noise with decreasing avalanche width. Moreover, this behaviour is found to be independent of the initiating carrier type, suggesting a disparate ionisation ratio is no longer necessary to ensure low avalanche noise.

Acknowledgments: This work was supported in part by EPSRC (UK) under grant GR/J49549; K.F. Li and D.S. Ong are supported by the University of Sheffield under studentships.

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Electronics Letters Online No: 19980021
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References

Optical responses of InGaP/GaAs/InGaAs P-channel double heterojunction pseudomorphic MODFET

The authors report on the optical responses of a p-channel InGaP/InGaAs/GaAs pseudomorphic MODFET with a gate length of 1.0 \mu m. The photocurrent of the device is \( 0.36 \mu A \) at \( V_g = -0.2 V \) and \( V_d = -3.5 V \), with incident optical power of 2.15 mW. A significantly high responsivity was obtained at low incident optical power range. Current gain cut-off frequency and maximum available gain cut-off frequency were increased by 20 and 10\%, respectively, under optical illumination.

P-channel modulation-doped field-effect transistors (MODFETs) have been under active study as a high speed, low power, dissipation complementary logic circuit with an n-channel MODFET [1]. Recently, the optical responses of n-channel MODFET devices, which have been found to be very useful in the area of high speed optoelectronic communications, have been reported [2, 3]. However, optical responses of p-channel MODFETs have not yet been reported. In this Letter, the optical characteristics of a p-channel InGaP/InGaAs/GaAs pseudomorphic MODFET grown on a GaAs substrate are reported for the first time.

In this Letter, we propose a symmetrically InGaP/InGaAs/InGaAs p-channel double heterojunction pseudomorphic MODFET. Employing InGaP/GaAs, which has a higher bandgap of 1.89 eV, we expect to have better carrier confinement owing to a
higher valence band offset and improved carrier transport of two-dimensional hole gas in the channel. The epitaxial layers were grown by gas source MBE on a GaAs substrate, and include an undoped GaAs (2000 Å) layer, a p-type In_{0.3}Ga_{0.7}As acceptor layer (100 Å, Be; 2 x 10^{18}cm^{-2}), an undoped In_{0.3}Ga_{0.7}As spacer layer (50 Å), an undoped GaAs spacer layer (50 Å), an undoped In_{0.3}Ga_{0.7}As channel layer (100 Å), an undoped GaAs spacer layer (50 Å), an undoped In_{0.3}Ga_{0.7}As spacer layer (50 Å), a p-type In_{0.3}Ga_{0.7}As acceptor layer (100 Å, Be; 2 x 10^{18}cm^{-2}), an undoped In_{0.3}Ga_{0.7}As cap layer (300 Å, Be; 3 x 10^{18}cm^{-2}). Hall mobility and a density of 2-DHIG in the pseudomorphic In_{0.3}Ga_{0.7}As channel at 300K were measured to be 250cm^2/Vs and 1.9 x 10^{11}cm^{-2}, respectively.

The fabricated pseudomorphic p-channel MODFET has a T-shaped gate structure with a gate length (L_g) of 1μm, a gate width (W_g) of 240μm, gate-source spacing (L_{gs}) and gate-drain spacing (L_{gd}) of 1.5μm. Devices were fabricated using a wet etching process with Au-Zn/Ge/Au for ohmic contact and Ti/Au for Schottky contact. We also used a selective etching process during gate recess to obtain better thickness control. PECVD-grown silicon nitride (1000 Å) was deposited for the passivation of fabricated devices before characterisation.

![Graph](image)

Fig. 1 Drain current-voltage characteristics of p-channel pseudomorphic MODFET

Incident optical power P_{opt} = 2.15mW, with V_{gs} = -0.2 to 1V (step = 0.4V)
- dark
- 2.15 mW

A Z = 800nm continuous laser diode source, an HP 4156A semiconductor parameter analyser, and an HP 8510B network analyser have been used to measure the optical characteristics of the fabricated In_{0.3}Ga_{0.7}As/In_{0.3}Ga_{0.7}As p-channel MODFET. The optical source was routed via an optical fibre (cleaved multimode fibre, minimum illumination diameter of 25μm, numerical aperture of 0.275) to the p-channel MODFET by bringing the fibre end into close proximity with the device’s surface so that the light spot covers the entire active area of the device under test (~200μm in diameter). Microwave scattering parameters were obtained from the device on wafer via an HP 8510B network analyser over a range of frequencies from 45MHz to 10GHz after calibration using the short-open-load-thru method. The drain-current-voltage characteristics are shown in Fig. 1 with incident optical power (P_{opt}) of 2.15mW. We obtained maximum drain-source saturation current without optical illumination: I_{dss} = -5.6mA with V_{gs} = 0.2V and V_{ds} = -3.5V. Conversely, we obtained I_{dss} = -5.96mA with the same bias conditions under optical illumination with P_{opt} = 2.15mW. The photocurrent I_m defined as I_{opt} - I_{dss} was, therefore, -0.36mA. In the saturation mode of the operation, the photocurrent with optical illumination shows almost independent of V_{gs}, for a given drain bias. However, photocurrent changes with drain-source voltage for fixed gate-source voltage.

The optical performance of the p-channel MODFET is also characterised by the responsivity defined as the photocurrent divided by the incident optical power. The responsivity against incident optical power is shown in Fig. 2 with V_{gs} = 0V and V_{ds} = 1V at V_{gs} = -3.5V, respectively. The responsivity of the p-channel MODFET is also better than that of a standard pin photodiode [2]. A significantly high responsivity is obtained at low incident optical powers, and it saturates with an increase in the incident optical power. The different responsivities at the gate-source voltage of 0 and 1V are due to the change in the photoemissive region of the p-channel MODFET, which is related to the photo-voltaic effect.

![Graph](image)

Fig. 2 Responsivity of p-channel MODFET against incident optical power for V_{gs} = -3.5V
- V_{gs} = 0V
- V_{gs} = 1V
- data of pin photodiode included for comparison [2]

![Graph](image)

Fig. 3 Current gain and maximum available gain against frequency curve with V_{gs} = 0.8V and V_{ds} = -3.5V with dark and incident optical power of 2.15mW
- dark
- 2.15 mW
- V_{gs} = -3.5V, V_{ds} = 0.8V

Due to the photo-voltaic and photoconductive effects, the characteristic parameters of the p-channel MODFET change the S-parameters of the intrinsic device. Current gain and maximum available gain versus frequency with V_{gs} = 0.8V and V_{ds} = -3.5V are shown in Fig. 3. The measurement was carried out with dark and incident optical power of 2.15mW, respectively. Under the optical illumination, current gain cut-off frequency (f_m) and maximum available gain cut-off frequency (f_m) were improved near
the pinch-off mode of operation, and found to be 2.11 and 4.06 GHz, respectively. Under optical illumination $I_{ph}$ was increased by 20%, while $I_{dark}$ was improved by 10% compared with microwave performance under non-illumination.

In summary, a $p$-channel InGa$_x$GaAs$_{1-x}$/P/GaAs/InGa$_x$GaAs$_{1-x}$ pseudomorphic MODFET with 1µm gate length has been fabricated. DC and microwave performance of the devices were characterised with and without optical illumination. We observed that the photocurrent was $-0.36$ mA at $V_g = -0.2$ V and $V_d = -3.5$ V with incident optical power of 2.15 mW. A significantly high responsivity was noted at low incident optical powers. Under the optical illumination, current gain cut-off frequency and maximum available gain cut-off frequency were improved. These results of the optical responses of the $p$-channel InGa$_x$GaAs$_{1-x}$/P/GaAs/InGa$_x$GaAs$_{1-x}$ pseudomorphic MODFET on a GaAs substrate are reported for the first time.

References


Suppression of boron penetration in $p^*$ poly-Si gate using Si-B diffusion source

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The authors report a novel Si-B diffusion source for doping $p^*$-poly-Si gates in pMOSFETs. It is found that B penetration can be effectively suppressed by using this novel process. All of the electrical properties of the MOS capacitors are significantly improved over those in the conventional BF$_2^+$ or B$^+$-implanted samples. This new process is very promising for future surface-channel pMOSFETs.

Introduction: $p^*$-polycrystalline silicon ($p^*$-poly-Si) has been proposed as the gate material for surface-channel $p$-type metal-oxide-semiconductor transistor (pMOSFET) in deep submicron complementary metal-oxide semiconductor devices [1]. This is because surface-channel pMOSFETs using $p^*$-poly-Si gates have better short-channel and sub-threshold I-V characteristics. They also exhibit improved controllability of the threshold voltage over buried-channel pMOSFETs with an $n^+$-poly-Si gate. However, the fast boron diffusion in the poly-Si and gate oxide, results in the susceptibility of boron penetration through the gate into the underlying silicon substrate. The presence of F, due to BF$_2^+$ implantation, further enhances the diffusion of B [2]. Boron penetration is known to cause device instability such as positive threshold voltage shift, increased subthreshold swing, increased electron trapping rate, low-field hole mobility degradation, and drive current degradation due to poly-Si depletion in pMOSFETs. Many methods have been proposed to suppress boron penetration. The first approach is to retard the boron diffusion in the poly-Si. This can be achieved by stacked or modified poly-Si gate structures [3]. The second approach is to establish a diffusion barrier at the interface of the poly-Si/oxide and/or oxide/Si-substrate. This can be achieved by nitridation of the gate and/or gate oxide by using N$_2$O or NO oxidation/annealing, or an inductive-coupling-nitrogen-plasma to incorporate a nitrogen-rich layer at the SiO$_x$/Si interface as a barrier to retard the boron diffusion [4]. In this Letter, a novel Si-B layer is proposed, for the first time, as the diffusion source for doping the $p^*$-poly-Si. The comprehensive effects of annealing temperature and time on the $p^*$-poly-Si MOS capacitors using a Si-B layer are compared with the conventional BF$_2^+$ and B$^+$-ion-implanted counterparts by using secondary ion mass spectroscopy (SIMS) analyses, high-low frequency C-V measurements, J-E characters, and charge-to-breakdown ($Q_{cb}$) values. It is found that this new process, which is inherently free of F, has a better capability for suppressing boron penetration than conventional methods employing either BF$_2^+$ or B$^+$ implantation.

![Flat-band voltage of BF$_2^+$-implanted, B$^+$-implanted and Si-B samples annealed at 875–950°C for 15min](image1)

**Fig. 1** Flat-band voltage of BF$_2^+$-implanted, B$^+$-implanted and Si-B samples annealed at 875–950°C for 15min

- Si-B
- B$^+$
- BF$_2^+$

![Distribution of charge-to-breakdown of BF$_2^+$-implanted and Si-B samples](image2)

**Fig. 2** Distribution of charge-to-breakdown of BF$_2^+$-implanted and Si-B samples

- 875°C
- 900°C
- 925°C
- 950°C

Experiment: $p^*$-poly-Si gate MOS capacitors were fabricated on n-type (100) Si-wafer with from 2 to 4Ω cm resistivity. The active area was defined with 550nm of field oxide. A thin 9.5nm gate oxide was grown at 900°C. A 300nm poly-Si was then deposited. Samples with the conventional implanted $p^*$-poly-Si gate were fabricated by using BF$_2^+$, 50keV, or B$^+$, 20keV, both to a dose of 5 x 10$^{14}$/cm$^2$; while for the Si-B samples, they were put instead into a ultra-high-vacuum vapour chemical deposition (UHVCVD) system to deposit a 35nm Si-B layer upon the undoped poly-Si gate layer by using a 1:1 mixture of pure SiH$_4$ and B$_2$H$_6$ (1% in H$_2$) at 550°C. The base pressure was 2 x 10$^{-4}$ torr. Afterwards, all samples were annealed in wet O$_2$ ambient at temperatures between 875 and 950°C for 15-35min. The Si-B layer was oxidised during