\( V_{GS}/V_{DS} \) Configuration-Dependence of Positive Bias Stress-Induced Instability in Self-Aligned Top-Gate IZO TFTs

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Since mass production of the oxide thin-film transistor (TFT)-driven backplanes in active-matrix organic light-emitting diode (AMOLED) displays began very recently, detailed understanding of instability in oxide TFTs under AMOLED operation condition has become indispensable for successful commercialization of oxide emitting diode (AMOLED) displays. In this work, the current-flowing stress-induced instability is investigated in the self-aligned top-gate indium-zinc-oxide (IZO) TFTs and the related mechanisms are discussed with two different \( V_{GS}/V_{DS} \) configurations, i.e., a high \( V_{DS} \) (HVDS, \( V_{GS}/V_{DS} = 10V/30V \)) and high \( V_{GS} \) (HVGS, \( V_{GS}/V_{DS} = 30V/10V \)) stress conditions. The subgap density-of-states (DOS) was traced during the stress time by using the multifrequency C-V method. As the stress time increased, the frequency-dispersion of C-V characteristics and the shift of threshold voltage (\( \Delta V_T \)) became prominently different from each other with varying \( V_{GS}/V_{DS} \) configurations [Fig. 1(a), (b)]. In comparison with HVGS, both generation of deep trap and the annihilation of shallow trap were clearly observed only in HVGS condition [Fig. 1(c), (d)]. This finding was consistent not only with the positive \( V_{GS}/V_{DS} \) stress time-evolutions of I-V and C-V characteristics, but with the \( V_{GS}/V_{DS} \) configuration-dependence as well.

**Fig. 1.** (a) Capacitance-voltage curves and (b) \( \Delta V_T \). The stress time evolutions of DOS in (c) HVDS and (d) HVGS conditions.

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