A NOVEL ANALYTICAL MODEL FOR SHORT CHANNEL HETEROSTRUCTURE FIELD EFFECT TRANSISTORS

SANG-HO SONG and DONG MYONG KIM
School of Electrical Engineering, Kookmin University, 861-1 Jungnang-dong, Sungbuk-gu, Seoul, 136-702, South Korea

(Received 16 July 1997; in revised form 7 October 1997)

Abstract—In this paper, we propose a novel analytical model for accurate and efficient simulation of integrated circuits with short channel heterostructure field effect transistors (HFETs). The proposed model for short channel HFETs is based on an analytical expression of the voltage-dependent two-dimensional electron gas density, which is either a linear or logarithmic function of the gate voltage. This compact model accurately describes the electrical characteristics of HFETs over the whole operation range including linear, saturation, and subthreshold operation without any discontinuity, which is known to be a detrimental factor for accurate modeling and simulation of analog and digital integrated circuits with field effect transistors. This new compact model has been verified with experimental data obtained from an Al$_{0.7}$Ga$_{0.3}$As/GaAs/In$_{0.17}$Ga$_{0.83}$As double heterojunction pseudomorphic HFET with a gate length $L_g = 1$ μm. © 1998 Elsevier Science Ltd. All rights reserved.

1. INTRODUCTION

A compact and accurate model for heterostructure field effect transistor (HFET) is very important as a CAD tool for the efficient and accurate simulation of digital, analog, and mixed-mode integrated circuits for both high-speed and high-frequency applications[1]. In particular, continuity over the full bias range, including the linear, saturation, and subthreshold region, in the current-voltage characteristics of the HFET is very important for accurate simulation of ICs. There are useful models for field effect transistors, such as BSIM3v3 and Philips model 9, for improved accuracy with compactness in the modeling and simulation of insulated gate FETs over all operation regions[2-4]. However, even though they are widely used in high performance CAD tools for large scale integrated circuits and systems they are rather complicated. In addition, those models require a significant number of characteristic parameters for precise description of the electrical performance. Furthermore, most of previously reported HFET models are semi-empirical and some model parameters lack a physical meaning causing a very long CPU time for the simulation of high density integrated circuits. In some cases, they use complicated smoothing functions for better fitting of the measured electrical characteristics without carrying any physical correlation.

In this paper we discuss a novel physics-based analytical dc model, with compactness and continuity over all operation regions, for better description and more efficient simulation of short channel HFETs keeping a high accuracy in the simulation of HFET integrated circuits. The proposed model for the HFET is based on an analytical expression of the voltage-dependent two-dimensional electron gas density, which is either a linear function under large applied voltage or a logarithmic function under low bias. The nonlinearity of the carrier concentration under large gate voltage, which is caused by partial ionization and partial depletion of the wide bandgap donor layer, is neglected in this model for compactness and accuracy of the model.

Both under subthreshold and above-threshold operation, the proposed model accurately describes the electrical characteristics of HFETs over the whole operation range including the linear and saturation region without discontinuity, which is known to be a detrimental factor for accurate modeling and simulation of analog and digital integrated circuits with field effect transistors. We also expect that the proposed model can be extended to the MOSFET considering the similarity in the operation of HFETs and MOSFETs[5].

We have also verified the validity and accuracy of the proposed HFET model with experimental data obtained from an Al$_{0.7}$Ga$_{0.3}$As/GaAs/In$_{0.17}$Ga$_{0.83}$As GaAs/Al$_{0.7}$Ga$_{0.3}$As HFET. The proposed HFET model presents an accurate description of the current-voltage characteristics over all operation regions without discontinuity and smoothing function even though the compared device has a pseudomorphic double heterostructure on a GaAs substrate.
2. MODELING OF HETEROSTRUCTURE FIELD EFFECT TRANSISTORS

2.1. Modeling of two-dimensional channel carriers in HFETs

The concentration \( n_c \) of the two-dimensional electron gas (2-DEG) in the n-channel HFET, which is the basis of the model, depends on the difference between quantized energy levels \( E_{0n} \) and quasi-Fermi level \( E_{F1n} \) for electrons. It can be described by [6]

\[
n_c = D\zeta V_{th} \ln \left[ 1 + \exp \left( \frac{E_{F1n}(n_c) - E_{0n}(n_c)}{kT} \right) \right]
\times \left[ 1 + \exp \left( \frac{E_{F1n}(n_c) - E_{0n}(n_c)}{kT} \right) \right],
\]

where \( D \) is defined as the density of allowed states in the conducting channel considering a finite two-dimensional quantum well in the heterostructure. Although there are other higher quantized energy levels it is well known that the density of 2-DEGs in the HFETs is predominantly limited by the quantized energy level \( E_{0n} \). Therefore, in order to build a compact model without losing accuracy we introduce a fill factor \( \zeta \) for the contribution of the first quantized energy level \( E_0 \). With this trade-off between accuracy and compactness, the two-dimensional channel carrier concentration \( n_c \) can be simplified to [7-9]

\[
n_c = D\zeta V_{th} \ln \left[ 1 + \exp \left( \frac{E_{F1n}(n_c) - E_{0n}(n_c)}{kT} \right) \right]
\equiv D_{eff} V_{th} \ln \left[ 1 + \exp \left( \frac{E_{F1n}(n_c) - E_{0n}(n_c)}{kT} \right) \right],
\]

with the fill factor \( \zeta \) and the effective density of states \( D_{eff} \) being defined as

\[
D_{eff} = D\zeta.
\]

where

\[
\zeta = 1 + \ln \left[ 1 + \exp \left( \frac{E_{F1n}(n_c) - E_{0n}(n_c)}{kT} \right) \right]
\times \frac{1}{\ln \left[ 1 + \exp \left( \frac{E_{F1n}(n_c) - E_{0n}(n_c)}{kT} \right) \right]}.
\]

The contribution of the first quantized energy level \( E_1 \) to the channel carrier concentration has been accommodated into the effective density of states \( D_{eff} \) by the channel fill factor \( \zeta \). The channel fill factor \( \zeta \) can be assumed to be either 1 for compactness of the model under moderate bias conditions or can be fully considered for better accuracy of the model taking into account both \( E_0 \) and \( E_1 \) at the bias condition of the HFETs.

We also adopt a capacitive channel coupling factor \( \eta \) and a gate-to-channel voltage \( V_{GS} \) under the assumption that only part of the gate voltage \( V_{GS} \) contributes to the formation of mobile channel carriers due to the multiple epitaxial layer in HFETs. In order to model the above modulation effect on the density of 2-DEGs by \( V_{GS} \), we define the energy \( \phi_{n} \) as the difference between the quasi-Fermi level and the ground quantized level. It can be described as a function of bias-dependent capacitances \( C_g \) and \( C_{ch} \), which is related to the channel coupling factor, and has been described in [10]

\[
\phi_n = E_{F1n} - E_{0n} \approx E_{F1n} + \frac{q}{1 + C_{ch}(V)/C_g(V)} \frac{1}{V}
\]

\[
\phi_n = E_{F1n} + \frac{q}{\eta(V)} V.
\]

In which \( C_{ch} \) is the channel capacitance and \( C_g \) is the capacitance of the wide bandgap carrier supply layer as shown in Fig. 1. The capacitive channel coupling factor \( \eta \) between the gate and the channel depends on the thickness \( t \) and the permittivity \( \varepsilon \) of the wide bandgap donor layer \( (d) \) and the intrinsic spacer layer \( (d) \).

In addition, the capacitive channel coupling factor \( \eta \) is also modulated by the drain voltage and can be modeled by an empirical formula with zero-bias \( (V_{DS}=0) \) coupling factors \( \eta_0 \) and \( \beta \) according to

\[
\eta = \eta_0 (1 + \beta V_{DS}).
\]

The characteristic parameter \( \beta \) \( (V^{-1}) \) models the \( V_{DS} \)-dependence of the coupling factor on the 2-DEG allowing modulation of both the quasi-Fermi
level and the channel carrier density with drain bias[9].

We can also simplify the HFET model using the Fermi level $E_{FV}$, which is completely dependent on the epitaxial structure, under thermal equilibrium. It is described by

$$E_{FV} = \left\{ q\phi_{ns} - \frac{q^2 N_d d_3}{2\varepsilon} - \Delta E_c + E_{Fmatter}(T) \right\},$$  

(7)

and depends on parameters of the epitaxial layer structure of the HFET ($\phi_{ns}$ is the workfunction difference; $\Delta E_c$ the conduction band discontinuity; $d$ the thickness and $N_d$ the doping).

As a function of the applied voltages ($V_{GS}$ and $V_{DS}$) through the capacitive channel coupling $\eta$, we finally obtain the channel carrier density $n_c$ as

$$n_c(V) = \frac{q\eta}{\eta q} \ln \left[ 1 + \exp \left( \frac{qV + qE_{FV}}{\eta q} \right) \right]$$  

(8)

using the threshold voltage $V_T (= -qE_{FV}/\eta q)$ and the thermal voltage $E_{Fq} (= kT/q)$.

The channel carrier density $n_c$ is a logarithmic function of the channel potential at very low gate voltage (the subthreshold operation) while it is a linear function under significantly high gate bias (above threshold operation). Depending on the voltages applied to the gate and the drain this compact model fully covers both sub- and above-threshold regions. This result agrees well with previously reported experimental observations for the bias-dependent carrier concentration.

2.2. The current voltage characteristics of the HFET in the linear region of operation

The total drain current ($I_{th}$) consists of four different current components which include drift and diffusion of both 2-DEGs controlled by the gate voltage and the bulk carrier charges supplied by the source. It is mainly determined by drift of the high density 2-DEG under large gate bias while it is limited by diffusion of free carriers from the source under low gate bias due to the extremely low density of the 2-DEGs. Therefore, the total charge contributing to the current flow can be described by

$$Q_{total} = Q_{2-DEG} + Q_{Sub}$$  

$$= \left( 1 + \frac{C_{ch}}{C_F} \right) Q_{2-DEG} = \eta Q_{2-DEG},$$  

(9)

where $Q_{2-DEG}$ and $Q_{Sub}$ represent the contribution of the 2-DEG and the contribution of bulk carriers from the source which limits the current at subthreshold operation of HFETs.

It is well known that the drain current in the subthreshold region, either in the linear mode or in saturation, depends exponentially on the gate bias and is limited by the diffusion (thermionic emission) process of carriers from the source overcoming the energy barrier to the channel. Therefore, the drain current generally can be obtained from the gradient of the quasi-Fermi level for electrons given by[10]

$$I_{th} = -q\eta E_{Fq} \frac{d\phi_{ns}}{dV} = -q\eta E_{Fq} \frac{d\phi_{ns}}{dV} \frac{dV}{dV} dx.$$  

(10)

Assuming a constant carrier mobility under small drain voltage in the linear region of HFET operation, the drain current can be described by

$$I_{th} = -q\eta E_{Fq} D_{eff} \int [1 + \exp \left( \frac{V - V_T}{\eta V_{th}} \right)] dV.$$  

(11)

where $W, L$ and $V$ mean the width, the gate length, and the gate-to-channel voltage, respectively.

Therefore, the drain current can be written as a function of the gate, drain, and threshold voltage according to

$$I_{th} = \frac{q^2 \eta E_{Fq} D_{eff} V_{th}^2}{L} \int_{V_s}^{V_t} \frac{1}{X - 1} \ln(X) dX$$  

$$= \frac{q^2 \eta E_{Fq} D_{eff} V_{th}^2}{L} \int_{\xi_t}^{\xi_s} \frac{1}{X - 1} \ln(X) dX$$  

(12)

introducing

$$\hat{X} = 1 + \exp \left( \frac{V - V_T}{\eta V_{th}} \right).$$  

(13)

and

$$\xi_s = \int_{X_s}^{X_t} \frac{1}{X - 1} \ln(X) dX \int_{X_s}^{X_t} \frac{1}{X - 1} \ln(X) dX.$$  

(14)

with boundary conditions for $X$ at the source and the drain given by

$$X_0 = 1 + \exp \left( \frac{V_{GS} - V_T}{\eta V_{th}} \right).$$  

(15)

and

$$X_1 = 1 - \exp \left( \frac{V_{GS} - V_{DS} - V_T}{\eta V_{th}} \right).$$  

(16)

respectively.

In the case of a large gate voltage above threshold forming a high density channel with $V - V_T > \eta V_{th}$ at small drain voltage, $\xi$ can be conveniently assumed to be 1. Even with $V_{th} = 26$ mV at $T = 300$ K, $V - V_T = 3V_{th} = 78$ mV is large enough to satisfy the above assumption within 5% of error. On the other hand for $(V - V_T) < \eta V_{th}$ at a very low channel field with a small drain bias, the drain current is very small and $\xi$ can again be replaced by 1. However, even in the subthreshold operation of HFETs with $(V - V_T) \ll \eta V_{th}$ and small drain bias, $\xi$ can be fully considered for better modeling of the subthreshold characteristics of HFETs for low gate voltages and Equation (13) can
be approximated by an exponential function with an appropriate logarithmic slope of the original function. This subthreshold slope can be easily modeled by adjusting the subthreshold slope factor ($\eta$) and $\xi$ in the HFET model. Therefore, we can use Equation (13) for modeling an HFET at small drain voltage over all regions without losing accuracy.

Therefore, we finally obtain for the drain current of the HFET in the linear region of operation

$$I_{Dlin} = \frac{qW\mu_n\xi D_{eff}V_{th}^2}{2L} \left[ \ln \left[ 1 + \exp \left( \frac{V_{GS} - V_{T}}{\eta V_{th}} \right) \right] \right]$$

$$- \ln \left[ 1 + \exp \left( \frac{V_{GS} - V_{DS} - V_{T}}{\eta V_{th}} \right) \right]$$

as a function of gate and drain voltages at both the subthreshold and above-threshold operation.

As shown above, the drain current in the linear region of operation can be simplified to the previously reported HFET models when both $V_{GS} - V_{T}$ and $V_{GS} - V_{DS} - V_{T}$ are larger than $\eta V_{th}$. Depending on the bias condition the current behavior in subthreshold condition can also be described well by modifying $\xi$ and $D_{eff}$.

2.3. The current–voltage characteristics of HFETs in the saturation region

With a large drain bias at a given gate voltage, there are two possible mechanisms for the saturation of the drain current. In the case of current saturation caused by pinch-off of the channel at the drain side under the gate with $V_{GD} < V_{T}$, which usually appears in short channel HFETs, the saturated drain current can be derived from the result obtained in the previous section for the linear region of operation.

In the other case of current saturation, due to saturation of carrier velocity at a high lateral electric field and usually appearing in a short channel FET, the saturated drain current $I_{DSat}$ can be obtained by using a drain saturation voltage ($V_{DS(max)} = V_{sat}$) and the saturated carrier velocity ($v_{sat}$) according to

$$I_{DSat} = qWD_{eff}V_{th}v_{sat} \ln \left[ 1 + \exp \left( \frac{V_{GS} - V_{sat} - V_{T}}{\eta V_{th}} \right) \right]$$

$$= qWD_{eff}V_{th}v_{sat} \times \ln \left[ 1 + \exp \left( \frac{V_{GS} - V_{sat} - V_{T}}{\eta V_{th}} \right) \right]$$

$$\times \exp \left( \frac{(V_{GS} - V_{sat} - V_{T})/\eta V_{th})}{1 + \exp \left( (V_{GS} - V_{sat} - V_{T})/\eta V_{th}) \right)} \right).$$

We use the above to obtain a compact analytical model satisfying continuity of current at $V = V_{sat}$, which is reached due to saturation of the carrier velocity in a short channel HFET. As described in the previous section, this assumption is reasonable for a small value of $V_{GDS(max)}$ ($\sim V_{th}$) for short channel HFETs operating at a high lateral electrical field for a large drain voltage. For continuity of the drain current model satisfying $I_{Dlin}(V_{sat}) = I_{DSat}(V_{sat})$ at $V_{DS} = V_{DS(max)}$, the saturated drain current should satisfy

$$I_{DSat} = qWD_{eff}V_{th}v_{sat}$$

$$\times \ln \left[ 1 + \exp \left( \frac{V_{GS} - V_{sat} - V_{T}}{\eta V_{th}} \right) \right]$$

$$\times \exp \left( \frac{(V_{GS} - V_{sat} - V_{T})/\eta V_{th})}{1 + \exp \left( (V_{GS} - V_{sat} - V_{T})/\eta V_{th}) \right)} \right) \times \frac{\mu_n\eta D_{eff}V_{th}^2}{2L} \ln \left[ 1 + \exp \left( \frac{V_{GS} - V_{T}}{\eta V_{th}} \right) \right]$$

$$- \ln \left[ 1 + \exp \left( \frac{V_{GS} - V_{sat} - V_{T}}{\eta V_{th}} \right) \right].$$

In order to obtain continuity of the HFET model between the linear and the saturation regions of operation, the saturated drain current can be modified introducing the quantities $Y$ and $Y_{o}$ defined as

$$Y = \ln \left[ 1 + \exp \left( \frac{V_{GS} - V_{sat} - V_{T}}{\eta V_{th}} \right) \right]$$

and:

$$Y_{o} = \ln \left[ 1 + \exp \left( \frac{V_{GS} - V_{T}}{\eta V_{th}} \right) \right].$$

From the above, we obtain

$$v_{sat} \frac{Y^2}{Y + 1} = \frac{\mu_n\eta V_{th}}{2L} (Y_{o} - Y^{2})$$

and

$$Y^2 + \left( \frac{2LV_{sat}}{\mu_n\eta V_{th}} \right) Y^2 - Y_{o}Y - Y_{o} = 0.$$

assuming $\epsilon^{\prime} \geq 1 + Y$ for small values of $Y$ at moderate gate bias conditions.

In the case of a large value of $Y$ at extremely high gate bias, there will be a significant change in the current–voltage characteristics due to the parallel conduction phenomenon by the transfer of electrons into the wide bandgap layers. This parallel conduction induces a detrimental degradation in the I–I characteristics of HFETs due to the action of a parasitic MESFET with poor transport properties in the doped wide bandgap spacer and donor layers. Furthermore, there is a significant gate leakage degrading the input resistance due to a forward bias Schottky diode. Both parallel conduction mechanisms and the contribution from deep levels in the wide bandgap donor layer deteriorates the electrical performance of HFETs. Therefore, the parallel conduction mechanism and other effects caused by the carrier transferred into the wide bandgap layer at large gate voltage should be
avoided in normal operation and they have been excluded in the model.

Solving the above equation for \( V_T \), the drain voltage \( V_{sat} \) at current saturation is given by

\[
V_{sat} = V_{GS} - V_T - \eta V_{fb}
\]

\[
\times \ln \left[ 2\sqrt{Q} \cos \left( \frac{\theta}{2} \right) - \frac{1}{2} \left( 1 + \frac{2V_{sat}}{\mu_e V_{fb}} \right) \right] - 1
\]

(24)

where \( Q, R \) and \( \theta \) are defined as

\[
Q = \frac{3Y_v + (1 + 2L_{sat}/\mu_e V_{fb})^2}{9}
\]

(25)

\[
9Y_v(1 + 2L_{sat}/\mu_e V_{fb}) - 27Y_v
\]

\[
R = \frac{-2(1 + 2L_{sat}/\mu_e V_{fb})^3}{54}
\]

(26)

and

\[
\cos \theta = \frac{R}{\sqrt{-Q^3}}
\]

(27)

respectively.

For large drain voltages with \( V_{GS} < V_T \), the saturated drain current \( I_{sat} \) agrees well with the expression of previous conventional HFET models. The latter also applies to the current voltage characteristics in the subthreshold region.

2.4. Secondary effects in the HFET model

In the proposed model, secondary effects, such as channel length modulation, DIBL effect, and charge sharing effects, can be included for better modeling of the short channel, high performance HFETs. By solving the two-dimensional Poisson equation, the effective channel length modulation by the drain voltage can be modeled and the channel length \( L \) in the current equation of the proposed model has to be replaced by \( L_{eff} \) defined as[11]

\[
L_{eff} = L_0 - \frac{2d}{\pi} \sinh^{-1} \left[ \frac{\pi(V_{GS} - V_{sat})}{2d_{crit}} \right]
\]

(28)

where \( L_0 \) and \( d_{crit} \) mean the zero-bias gate length and the critical electrical field for velocity saturation.

The DIBL effect and the charge sharing effect in the short channel HFETs, which dominantly affect the two-dimensional carrier density responsible for the drain current, can be taken into account as a threshold voltage shift linear to the drain voltage with an empirical parameter \( z \)[8]

\[
V_T = V_{T0} - zV_{DS}
\]

(29)

The above secondary effects have also been implemented in the proposed HFET model by replacing the threshold voltage \( V_T \) with \( V_{T0} - zV_{DS} \).

3. SIMULATION RESULTS AND EXPERIMENTAL VERIFICATION

In order to verify the accuracy of the model proposed in this paper, we used an n-channel double heterostructure \( \text{Al}_{0.5}\text{Ga}_{0.5}\text{As-GaAs-In}_{0.5}\text{Ga}_{0.5}\text{As} \) pseudomorphic HFET grown by GSMBE on a semi-insulating (100)-GaAs substrate. The structure of the fabricated pseudomorphic HFET is shown in Fig. 2. We considered a double heterojunction quantum well structure to get better confinement and better carrier transport properties in the pseudomorphic InGaAs/GaAs channel layer. At room temperature from Hall measurements we obtained \( n_0 = \frac{5000 \text{ cm}^2}{\text{V} \cdot \text{s}} \) and \( n_s = 1.2 \times 10^{12} \text{ cm}^2 \) for 2D channel electrons.

We used Au/Ge/Ni/Au for n-type ohmic contacts and Ti/Al for the Schottky gate contact. V-shaped gate with \( L_x = 1 \mu \text{m} \), \( L_y = 1 \mu \text{m} \), and \( W = 240 \mu \text{m} \) has been made employing a selective wet etching process for a better control of the thickness of the pseudomorphic HFET. In case of experimental verification, the thickness of the channel was controlled by making use of the fabricated pseudomorphic HFET instead of a single heterostructure device. In order to achieve better carrier confinement and better transport properties of carriers in the channel, the advanced HFETs for improved transconductance and cut-off frequencies require a much more complicated epitaxial structure than a single heterojunction HFET. However, the proposed HFET model is still effective as far as the epitaxial layer of HFETs is properly designed and operated within parallel conduction phenomenon caused by carriers remaining in the N-AlGaAs donor layers, especially in the bottom part of the wide bandgap AlGaAs donor layer. In addition, the proposed HEET model has more flexibility in the application and can be applied to other modified epitaxial HFET structures by simply adjusting the channel fill factor \( \zeta \), the channel coupling factor \( \eta \).

<table>
<thead>
<tr>
<th>Material</th>
<th>Doping [cm(^{-3})]</th>
<th>Thickness [Å]</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs</td>
<td>n-type 5 \times 10(^{17}) (Si)</td>
<td>300</td>
</tr>
<tr>
<td>Al(<em>{0.5})Ga(</em>{0.5})As</td>
<td>Undoped</td>
<td>50</td>
</tr>
<tr>
<td>Al(<em>{0.5})Ga(</em>{0.5})As</td>
<td>N-type 1 \times 10(^{17}) (Si)</td>
<td>100</td>
</tr>
<tr>
<td>Al(<em>{0.5})Ga(</em>{0.5})As</td>
<td>Undoped</td>
<td>50</td>
</tr>
<tr>
<td>GaAs</td>
<td>Undoped</td>
<td>50</td>
</tr>
<tr>
<td>In(<em>{0.5})Ga(</em>{0.5})As</td>
<td>Undoped</td>
<td>100</td>
</tr>
<tr>
<td>GaAs</td>
<td>Undoped</td>
<td>50</td>
</tr>
<tr>
<td>Al(<em>{0.5})Ga(</em>{0.5})As</td>
<td>Undoped</td>
<td>50</td>
</tr>
<tr>
<td>Al(<em>{0.5})Ga(</em>{0.5})As</td>
<td>N-type 1 \times 10(^{17}) (Si)</td>
<td>100</td>
</tr>
<tr>
<td>GaAs</td>
<td>Undoped</td>
<td>2000</td>
</tr>
</tbody>
</table>

Fig. 2. The epitaxial HFET structure used in the verification of the proposed model.
\( \xi \) and other model parameters introduced in the above model.

For a verification of the accuracy of the proposed HFET model, crucial parameters for the Al\(_{0.3}\)Ga\(_{0.7}\)As/GaAs/In\(_{0.13}\)Ga\(_{0.87}\)As pseudomorphic HFET have been summarized in Table 1. The experimental data and the modeled electrical characteristics are given in Figs 3 and 4 for \( I_D-V_{DS} \) and \( I_D-V_{GS} \), respectively. Note that the proposed model makes use of only 12 model parameters over the full bias range. The average error in the linear and saturation region is less than 5%. The above model, with a minimum number of model parameters, is as accurate as conventional HFET models with a significant number of model parameters[2,3]. As shown in Fig. 5, we also verified the validity and accuracy of the proposed model examining continuity between different regions of operation, which is a most significant factor for the accuracy in analog and analog-digital mixed mode integrated circuit simulation. The transconductance \( g_m \) is given in the Fig. 5. The latter also gives good agreement with experimental data obtained from the pseudomorphic HFET.

### 4. CONCLUSION

We have proposed a novel analytical model for accurate simulation of integrated circuits with HFETs with a minimum number of model param-

---

**Table 1. Physical and material parameters used in the modeling and verification of the fabricated HFET**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Model values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Geometrical</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( L_g )</td>
<td>1</td>
<td>( \mu \text{m} )</td>
</tr>
<tr>
<td>( W )</td>
<td>240</td>
<td>( \mu \text{m} )</td>
</tr>
<tr>
<td>( d )</td>
<td>800</td>
<td>( \text{\AA} )</td>
</tr>
</tbody>
</table>

**Electrical**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Model values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( D_{ox} )</td>
<td>( 1.24 \times 10^{12} )</td>
<td>( \text{cm}^{-2} \text{V}^{-1} \cdot \text{s}^{-1} )</td>
</tr>
<tr>
<td>( \mu_n )</td>
<td>5000</td>
<td>( \text{cm}^2 \text{V}^{-1} \cdot \text{s}^{-1} )</td>
</tr>
<tr>
<td>( V )</td>
<td>-0.645</td>
<td>( \text{V} )</td>
</tr>
<tr>
<td>( \gamma )</td>
<td>0.02</td>
<td>( \text{cm}^{-2} \text{V}^{-1} \cdot \text{s}^{-1} )</td>
</tr>
<tr>
<td>( z )</td>
<td>0.035</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( R_e )</td>
<td>1</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( R_i )</td>
<td>10</td>
<td>( \Omega )</td>
</tr>
</tbody>
</table>

**Modeling**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Model values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( v_{sat} )</td>
<td>( 4.5 \times 10^3 )</td>
<td>( \text{cm} \cdot \text{s}^{-1} )</td>
</tr>
<tr>
<td>( \rho_{sat} )</td>
<td>9000</td>
<td>( \text{[V cm]} )</td>
</tr>
</tbody>
</table>

---

**Fig. 3.** Measured and simulated drain current-drain voltage characteristics \( (I_D-V_{DS}) \) of the HFET
Fig. 4. Measured and simulated drain current-gate voltage characteristics ($I_{ds}$–$V_{gs}$) of the HFET

parameters. The proposed model was derived from an analytical expression of the voltage-dependent two-dimensional electron gas density in terms of a linear or logarithmic function of the applied voltages. The model accurately describes the electrical characteristics of HFETs over all regions of operation including the linear, saturation, and subthreshold region without discontinuity, which is known to be a very important factor for accurate modeling and simulation of high performance analog and digital integrated circuits with HFETs or other field effect transistors. The accuracy and robustness of the pro-

Fig. 5. Measured and simulated transconductance as a function of drain current ($g_m/I_{ds}$–log($I_{ds}$)) showing continuity of the model over the whole bias range
posed HFET model has been verified with experimental data obtained from an Al_{0.3}Ga_{0.7}As/GaAs/In_{0.1}Ga_{0.9}As double heterojunction pseudomorphic HFET. In addition, we expect that the above model can be widely applied to HFETs with modified epitaxial structure by adjustable model parameters. Considering the similarity in the operation of MOSFETs the above model is expected to be applicable to silicon MOSFETs with a very small number of model parameters.

REFERENCES