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One Transistor–Two Memristor Based on Amorphous Indium–Gallium–Zinc-Oxide for Neuromorphic Synaptic Devices

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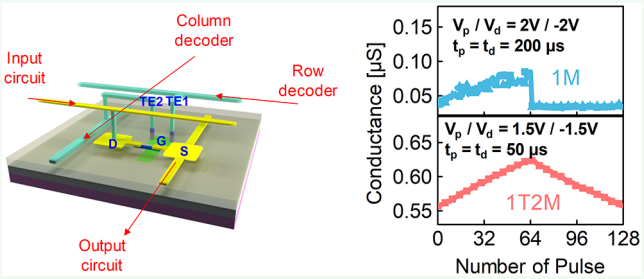
ABSTRACT: Various memristor-based synaptic devices have been proposed for implementing a neuromorphic system. However, memristor devices typically suffer from various inherent problems such as nonlinearity and asymmetry of conductance modulation and the sneak path issue of the crossbar array structure. To solve these drawbacks, we propose a one transistor–two memristor (1T2M) synaptic device, its array structure, and its operation method for neuromorphic system applications. For the channel of the transistor and switching layer of the memristor, amorphous InGaZnO was used. The proposed 1T2M synaptic device exhibited more linear and symmetric characteristics of conductance modulation compared with the single memristor device. In addition, the proposed array structure was robust to the sneak path problem. To investigate the switching mechanism, a depth profile analysis of X-ray photoelectron spectroscopy was conducted for each resistance state. Finally, we confirmed an excellent pattern recognition accuracy by using an artificial neural network simulation.



KEYWORDS: *amorphous InGaZnO, one transistor–two memristor synaptic device, linear/symmetric synaptic behavior, MNIST, neuromorphic*

INTRODUCTION

Modern computing systems are based on the von Neumann architecture, where the processing and memory units are physically separated from each other. In today's era of big data, however, conventional digital computers face a fundamental bottleneck in terms of performance and power efficiency. To address the von Neumann bottleneck, several solutions have been proposed at the device, circuit, and system levels. One of the promising approaches is a neuromorphic system that emulates the functionalities of the human brain.[1−7] To emulate the functionalities of biological synapses, various types of synaptic devices such as phase change,[8−12] resistance change,[13,14] ferromagnetic,[15,16] ferroelectric,[17−21] and field-effect transistor-based[19−22] have been proposed. Among them, memristors based on resistance changes have received great attention owing to their simple two-terminal structure, low energy consumption per neuronal activity, and analogue synaptic weight (conductance) modulation. Memristors can retain their internal conductance states depending on the history of the amount of charge flowing through them. These conductance states can be employed to emulate synaptic weights by using voltage as the input signal and current as the output signal.

To implement a neuromorphic system with low-power and high-speed operation, accurate cognitive task execution, and excellent reliability, various requirements for synaptic devices must be met. The preferred characteristics of traditional nonvolatile memories (NVMs), such as low operation energy, fast operation speed, good cycling endurance, long-term data retention, small variations (cycle-to-cycle and device-to-device), and small device size, are equally useful requirements for synaptic devices. Besides these, there are other requirements for synaptic devices. Most notably, synaptic devices require much higher multi-level precisions (>256 levels) than typical NVMs to achieve the desired learning accuracy.[23,24] As a result, most of the previous studies have focused on the development of analogue conductance modulation. In addition, the characteristics of conductance modulation are also important requirements. During the learning process of a neuromorphic system, the relationship between the device conductance and the number of programming pulses must be linear, and the rate at which the conductance increases (potentiation) and decreases (depression) should be sym-

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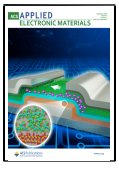

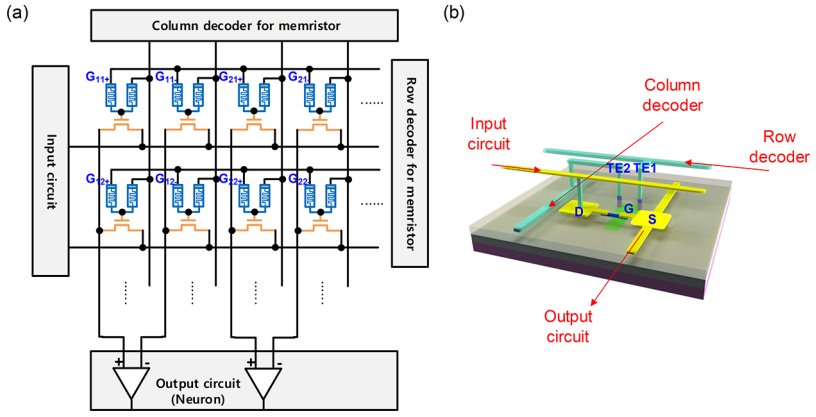

Figure 1. 1T2R synaptic (a) array configuration and (b) its device structure for a neuromorphic system.

metric for an accurate update of the synaptic weight. In general, however, most memristors still exhibit strongly nonlinear and asymmetric behavior on conductance modulation.[17,19] Several techniques have been proposed to address this problem.[18,25−28] To solve the nonlinearity problem, some researchers have utilized programming pulse modulation methods such as incremental pulse amplitudes or widths. However, these methods require a read-before-write (verification) operation to select the appropriating programming pulse, which consumes time and energy during the learning process of the neuromorphic system. Furthermore, it causes a significant burden on peripheral circuits. Therefore, the realization of linearity and symmetry at the device level would be a better solution. In this regard, several approaches using a combination of one transistor and two memristors (1T2M) have been proposed.[29] However, they require one select transistor or switch for each cell, which means that one synaptic device is a 2T2M rather than a 1T2M.

The resistance switching phenomena of memristors have been observed in various oxide-based materials, such as HfO*x*,[30−32] TiO*x*,[33−35] AlO*x*,[36,37] TaO*x*,[38,39] and ZnO.[40,41] Among them, amorphous indium−gallium−zinc oxide (IGZO) films have recently been found to show resistance switching behaviors.[42−45] Furthermore, IGZO is one of the most mature channel materials for thin-film transistors (TFTs) owing to its high carrier mobility, high transparency, flexibility, wide range of process temperatures, and high-yield process.[46−50] As IGZO can be used to make both transistors and memristor devices, neuromorphic systems can be manufactured without the complicated process needed to integrate neuron circuits and synaptic devices.

In this paper, we present one transistor−two memristor (1T2M) synaptic device and its array structure for the neuromorphic system. The proposed 1T2M devices were fabricated using IGZO as the channel material for the 1T and the switching material for the 2M. Compared with those of a one-memristor (1M) device, the linearity and symmetry of conductance modulation were improved. Based on the experimental data, we performed an artificial neural network simulation using the Modified National Institute of Standards and Technology (MNIST) database.

EXPERIMENTAL PROCEDURE

The IGZO-based memristor and transistor were fabricated as follows. We utilized a P^+-doped silicon substrate for the fabrication of the memristor and the transistor. P^+-Si substrates acted as the bottom electrode for the memristor and the gate electrode for the transistor.

For the fabrication of the memristor device, an amorphous IGZO film with a length of 80 nm was deposited by the radio frequency (RF) magnetron sputtering (150 W) deposition method in an Ar/O2 (3/2 sccm) atmosphere on the P^+-Si bottom electrode. Then, a 40 nm Pd layer was deposited onto the IGZO layer using e-beam evaporation and patterned to form the top electrode, which had an area of 100 × 100 μm^2.

The IGZO-based transistor (W/L = 50 μm/50 μm) was fabricated with the following sequence: First, a 50 nm SiO_2 film was formed on the P^+-Si substrate by the thermal oxidation process. Then, a 40 nm IGZO layer was deposited by the RF sputtering method with an Ar flux of 3 sccm and O_2 flux of 0.3 sccm. Finally, a 40 nm Ti layer for the source and drain region was deposited by e-beam evaporation with the aid of a metal shadow mask.

The atomic force microscopy (AFM) images of IGZO layer are shown in the Supporting Information, Figure S1.

The electrical properties of the fabricated devices were measured using a Keithley 4200 semiconductor parameter analyzer. X-ray photoelectron spectroscopy (XPS) analysis was performed using a Thermo Scientific K-Alpha spectrometer operated at 200 eV with a Al Kα radiation source.

RESULTS AND DISCUSSION

Figure 1 shows the 1T2M synaptic device structure and its array architecture. The two IGZO-based memristors were placed on the gate side of the IGZO-based transistor. By monolithically integrating two memristors on top of the transistor as shown in Figure 1b, the unit cell size is the same as one transistor size (10 F^2). Generally, memristor-based cross-point array architectures are susceptible to the sneak path problem.[51−53] In the proposed array architecture, however, input voltage signals and output current signals are applied to the transistors rather than the memristors. As a result, the device is robust to the sneak path problem. The specific operating principle of the proposed device is illustrated in Figure 2. The memristors on the right and left are denoted by M1 and M2, respectively. During the inference mode, the constant read voltages (V_{L_READ} and V_{R_READ}) are applied at the top electrodes of the two memristors (V_{TE1} and V_{TE2}) as depicted in Figure 2a. Currently, the two memristors serve as a voltage divider for the gate voltage (V_G) of the transistor and hence

$$V_G = V_{TE2} + (V_{TE1} - V_{TE2}) \times \frac{1}{1 + G_2/G_1} \quad (1)$$

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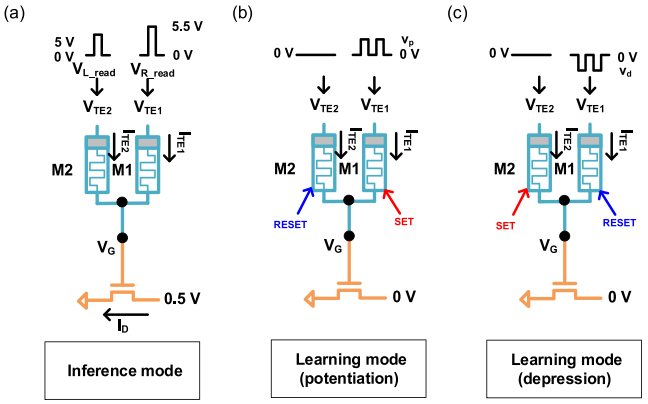

Figure 2. Operation principle of the 1T2M synaptic device: (a) inference operation method and learning operation methods for (b) potentiation and (c) depression.

where G_1 and G_2 are the conductance values of M_1 and M_2, respectively.

When the input voltage signal is applied at the drain node (V_D), the output current signal (I_D) is controlled by the gate voltage

$$I_D = \mu_{eff} C_{ox} \frac{W}{L} \times (V_G - V_T) \times V_D \quad (2)$$

where μ_{eff} is the effective mobility of the transistor, C_{ox} is the gate oxide capacitance, W is the effective channel width, L is the effective channel length, and V_T is the threshold voltage. We assume that the transistor operates in the linear region. Finally, the conductance (G) of the proposed 1T2M synaptic device can be obtained as follows

$$G = \mu_{eff} C_{ox} \frac{W}{L} \left[\left(V_{TE2} + (V_{TE1} - V_{TE2}) \times \frac{1}{1 + G_2/G_1} \right) - V_T \right] \quad (3)$$

Note that the conductance of the 1T2M synaptic device is determined by the conductance ratio (G_2/G_1) of the two memristors.

During the learning mode, a constant dc bias (V_{DC}) is applied to the top electrodes of M1 (TE1) and M2 (TE2), and the identical potentiation pulses (V_p) or depression pulses (V_d) are additionally applied to TE1 as shown in Figure 2b,c. At this time, the common bottom electrode voltage of M_1 and M_2 has an intermediate value between V_{TE1} and V_{TE2}, which are determined by eq 1. When the potentiation pulses (V_p) are applied at V_{TE1}, G_1 increases by the set operation of M_1 and G_2 decreases by the reset operation of M_2. Consequently, the conductance of the 1T2M synaptic device (G) increases. On the other hand, when the depression pulses (V_d) are applied at V_{TE2}, G_1 decreases by the set operation of M_1 and G_2 increases by the reset operation of M_2. Subsequently, G decreases. Note that both SET and RESET operations are used for potentiation or depression in the 2M devices. This is the basic principle of improving linearity and symmetry of the potentiation and depression. The details will be discussed later based on the results of the pulse response.

The memory characteristics of the individual memristor are shown in Figure 3. Initially, the forming process was carried out with a negative bias (−10 V) as shown in Figure 3a. Interestingly, after the forming process, the memristor was shown to be in the high-resistance state (HRS) and not the low-resistance state (LRS). After the forming process, the typical bipolar resistive switching is observed as illustrated in Figure 3b. The SET process occurs at a positive bias, while the RESET process occurs at the negative bias. During the measurement, the conduction current was limited by a compliance current of 1 mA to protect the device from a permanent breakdown.

By controlling the SET pulse, multi-level operation can be obtained as can be seen in Figure 3c. When we measured the conductance of the memristor with 0.5 V read pulses for 500 s, each conductance state is maintained without severe drift.

To analyze the resistive switching mechanism, an XPS analysis was carried. Figure 4a−c shows the O 1s XPS peaks at the near TE region, the middle region, and BE region, respectively. The O 1s peak can be categorized as having a metal−oxygen (M−O) bond of 530.2 eV, oxygen vacancy (V_o) of 531 eV, metal−hydroxide (M−OH) bond of 532 eV, and silicon−oxide (Si−O) bond of 533.4 eV.[54,55] Figure 4d−f illustrates the depth profile of the O 1s core level spectra when the device is in the as-fabricated (pristine) state, HRS (after forming or reset process), and LRS (after set process), respectively. The original O 1s spectra data along with the depth are shown in the Supporting Information, Figure S2. The XPS data reveal that the main switching operation of the memristor samples occurs near the Si bottom electrode. It is known that the native oxide at the Si bottom electrode of the pristine device is unstable owing to the ion bombardment effect by Ar plasma during the IGZO sputtering fabrication step.[56] As can be seen in Figure 4d, the Si−O peak at the bottom electrode is relatively high. This finding suggests that the bottom silicon oxide has a large Si dangling bond and that it is an insulating film. During the forming process, the oxygen ion (O^{2-}) migrates to the bottom electrode and forms a Si−O

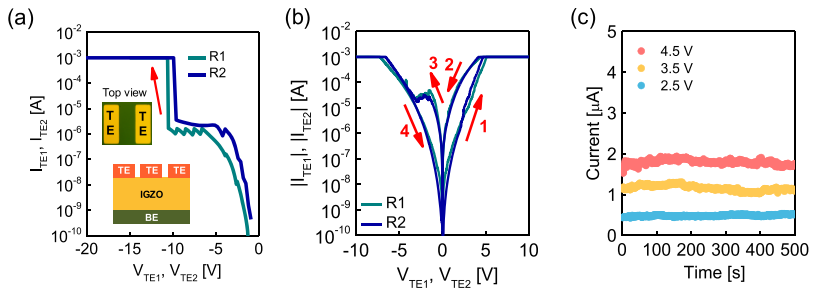

Figure 3. (a) Forming process of the fabricated memristor devices. (b) Bipolar resistive switching characteristics of the memristors. (c) Room-temperature state retention and read disturb of the memristor device.

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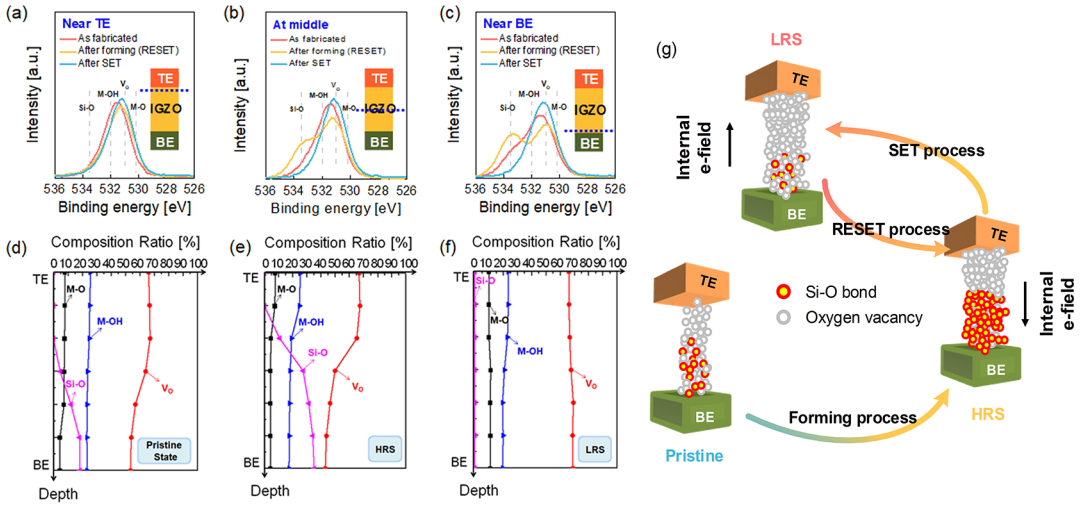

Figure 4. XPS profile of the O 1s core level: (a) XPS peaks near the TE region; (b) XPS peaks in the middle region; (c) XPS peaks near the BE region; (d) depth profile of the sample in the pristine state; (e) depth profile of the sample in HRS (after forming or reset process); (f) depth profile of the sample in LRS (after set process); and (g) schematic illustration of the switching mechanism in the Pd/IGZO/P$^+$-Si device.

bond (passivate the Si dangling bonds) at the Si interface. Subsequently, more stable silicon oxide is formed at the bottom electrode, and the device is in the HRS rather than an LRS after the forming process, as depicted in Figure 4e. Similarly, after the reset switching process, where a negative bias was applied to the top electrode, the device entered the HRS by the same mechanism as the forming process. On the other hand, during the set switching process, the oxygen ion migrates from the bottom electrode to the IGZO layer. Consequently, the number of Si−O bonds in the bottom region decrease. Conversely, the number of oxygen vacancies (V_o) increases at the bottom electrode and the IGZO layer, as depicted in Figure 4f. The Si dangling bond (also a kind of oxygen vacancy) at the bottom electrode and the oxygen vacancy in the IGZO layer form a conductive path, causing the device to enter the LRS. A schematic illustration of this switching process is depicted in Figure 4g.

The transfer characteristics and the output characteristics of the fabricated IGZO-based transistor are shown in Figure 5a,b, respectively. The fabricated transistor exhibits very little hysteresis in drain current versus gate voltage (Figure S3 in the Supporting Information).

Note that the transistor is operated in the linear region (V_D: 0−5 V) for the synaptic application. The mobility and the subgap density-of-states of the transistor were also extracted (Figure S5 in the Supporting Information).

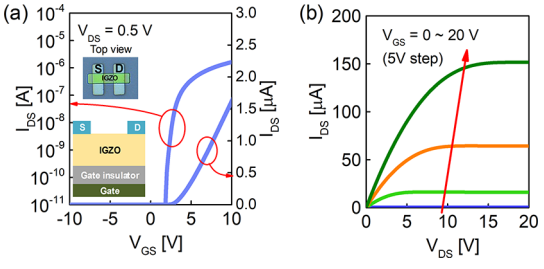

Figure 5. (a) Transfer characteristic (I_D−V_G) of the fabricated IGZO-based transistor. (b) Output characteristic (I_D−V_D) of the fabricated IGZO-based transistor.

For synaptic device applications, a gradual set and reset switching operation is essential. We evaluated the conductance modulation characteristics of the 1M device using a consecutive identical pulse scheme with positive amplitudes (V_p) for potentiation and negative amplitudes (V_d) for depression. Figure 6a−c shows the measured potentiation

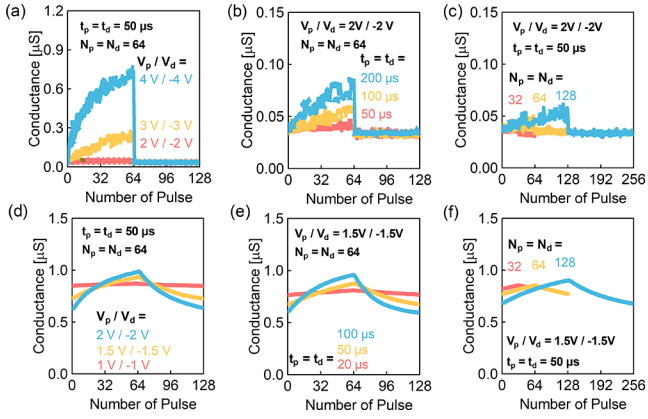

Figure 6. Potentiation and depression process of the 1M device under identical pulses with (a) three pulse amplitudes, (b) three pulse widths, and (c) different maximum number of pulses. Potentiation and depression process of the 1T2M device under identical pulses with (d) three pulse amplitudes, (e) three pulse widths, and (f) different the maximum number of pulses.

and depression curves of the 1M device. A read voltage of 0.5 V was used to measure the cell conductance. Figure 6a,b shows the conductance modulation with pulse amplitudes of V_p/V_d = 2/−2, 3/−3, and 4/−4 V, and with pulse widths of $t_p = t_d$ = 50, 100, and 200 μs. Figure 6c shows the conductance modulation characteristics along with the maximum number of applied pulses (N_p and N_d). The conductance change of the 1M device is not linearly proportional to the applied pulse number. The first few set or reset pulses causes a significant change, and the conductance change gradually saturates. During the reset operation, no further gradual conductance modulation was observed after the abrupt change with only the first pulse. This nonlinearity in the set and reset operation is similar to those

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reported in other memristor-based synaptic devices.[57−59] The switching mechanism of the Pd/IGZO/P$^+$-Si device is determined by oxygen ion migration as discussed earlier. At the first set pulse, oxygen ions are propelled rapidly from the bottom electrode toward the IGZO bulk and the top electrode by the applied electric field. At this time, the oxygen vacancy generated in the silicon oxide layer and the IGZO layer act as a conducting path, thus increasing the device conductance. When the oxygen ions accumulate in the top region of the IGZO layer, an internal electric field having an opposite direction to the applied electric field is generated, suppressing further oxygen migration toward the top interface. Therefore, the conductance change gradually decreases as the identical pulses are applied. On the other hand, the direction of the electric field generated by the applied negative voltage during the first reset pulse operation coincides with the direction of the internal electric field because of the space-charge effect of oxygen ion distribution. Therefore, one reset pulse causes the movement of more oxygen ions than the set pulse, indicating an abrupt reset modulation.

The conductance modulation characteristics of the 1T2M synaptic device are shown in Figure 6d−f. To modulate the conductance of the 1T2M device, identical potentiation or depression voltage pulses (V_p or V_d) were applied to the TE1 when a common dc bias of 5.0 V was applied to the TE1 and TE2. All of the conductance values were extracted by using a drain voltage of 0.5 V. Figure 6d,e shows the conductance modulation with pulse amplitudes of V_p/V_d = 1/−1, 1.5/−1.5, and 2/−2 V, and with pulse widths of $t_p = t_d$ = 20, 50, and 100 μs. Figure 6f shows the conductance modulation characteristics and the maximum number of applied pulses with a pulse amplitude of V_p/V_d = 1.5/−1.5 V and pulse width of $t_p = t_d$ = 50 μs. Compared with the 1M device, the 1T2M device exhibited improved linearity and symmetry of conductance changes. In particular, the initial abrupt conductance change in the reset process was effectively minimized. This improvement can be explained by eq 3. As explained earlier, both the SET and RESET operations are used for potentiation or depression in the 2M devices (potentiation: M1 set and M2 reset; depression: M1 reset and M2 set). The total conductance of the 1T2M device (G) is determined by the conductance ratio (G_2/G_1) of the two memristors. When depression pulses are applied during the depression operation, a reset operation and a set operation occurs in the M1 and M2 devices, respectively. Currently, even if the conductance of the M1 device (G_1) changes abruptly and becomes saturated, the conductance of the M2 device (G_2) gradually changes owing to the continuous set operation. Therefore, the entire conductance G can be gradually modulated without being saturated.

To quantitatively analyze the linearity and symmetry of the synaptic devices, we adopted the nonlinearity behavior model in the result of a previous work.[60] The conductance change with the number of pulses is given by the following equations

$$G_P = B \times \left[1 - \exp\left(-\frac{N}{A_p}\right)\right] + G_{min} \quad (4)$$

$$G_D = -B \times \left[1 - \exp\left(-\frac{N - N_{max}}{A_D}\right)\right] + G_{max} \quad (5)$$

$$B = \frac{G_{max} - G_{min}}{1 - \exp\left(-\frac{N_{max}}{A_p}\right)} \quad (6)$$

where G_{max} and G_{min} are the maximum conductance and minimum conductance, respectively, N_{max} represents the maximum pulse number needed to modulate the conductance between G_{min} and G_{max}, and B is simply a fitting parameter. The parameters A_P and A_D are the nonlinearity parameters of the potentiation and depression, respectively. A smaller absolute value of A_P or A_D indicates that the potentiation or depression characteristics are linear. In addition, as the absolute values of A_P and A_D are similar, the conductance modulation is symmetric. The characteristics of the 1M device and 1T2M device are summarized in Table 1.

Table 1. Comparison of the 1M and 1T2M Devices

	1M-1[a]	1T2M-1[b]	1M-2[c]	1T2M-2[d]
A_P	32	256	48	32
A_D	1	256	1	32
$G_{max}-G_{min}$	0.047 μS	0.067 μS	0.013 μS	0.329 μS

[a] V_p/V_d = 2/−2 V, $t_p = t_d$ = 200 μs. [b] V_p/V_d = 1.5/−1.5 V, $t_p = t_d$ = 50 μs. [c] V_p/V_d = 2/−2 V, $t_p = t_d$ = 50 μs. [d] V_p/V_d = 2/−2 V, $t_p = t_d$ = 50 μs.

Compared with the 1M device, 1T2M device exhibits improved linearity and symmetry. In addition, the 1T2M device has a larger total conductance window ($G_{max}-G_{min}$), which is another important advantage of the 1T2M device. This is because the inherent current amplification of the transistor, that is, the resistance ratio of the two memristors connected to the gate, is amplified by the transconductance (g_m) of the transistor to generate a drain output current. As the total conductance window increases, the margin between the conductance levels increases. Consequently, stable multi-level implementation is possible even with various unwanted variations.

The characteristics of memristor-based synaptic device structures are summarized in Table 2. 1T2M device can alleviate the sneak-path problem through a combination with the access transistor (1T). In addition, it has the same unit cell size as the 1T1M device by three-dimensional monolithically integration of memristors on top of a transistor. Linear conductance modulation can be obtained with the identical programming pulse scheme instead of programming pulse modulation schemes such as incremental amplitude or width, thereby eliminating additional read-before-write operations. 1T2M device-based array architecture requires additional metal lines and peripheral decoder circuitry. However, in general, this area is relatively small compared to the main array area. Therefore, the proposed 1T2M device configuration is a promising candidate for the memristor-based neuromorphic system.

To investigate the impact of nonlinearity and asymmetry of conductance modulation, on-chip learning simulation of pattern recognition was conducted using an MNIST hand-written data set. It is worth noting that the nonlinearity and asymmetry do not affect off-chip learning applications because the conductance of a synaptic device can be adjusted to a target level through an iterative program-verify scheme.[61,62] Conversely, in the case of on-chip learning, the program (potentiation or depression) pulses are applied to each

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Table 2. Comparison of the 1M, 1T1M, and 1T2M Device configuration

	unit cell size	sneak-path problem	programming pulse scheme for linearity	additional verify step before write	number of metal lines of array
1M	2 F^2	severe	incremental amplitude/width	required	2
1T1M	10 F^2 (transistor size)	Good	incremental amplitude/width	required	3
1T2M (this work)	10 F^2 (transistor size)	Good	identical pulse	not required (saving time and energy)	4

synaptic device without the verification step. At this time, the number of pulses to be applied is determined by the output current of the corresponding neuron circuit at the end of each column of the synapse array. As depicted in Figure 7a, we used

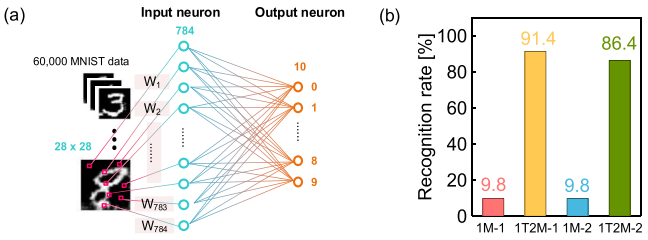

Figure 7. Comparison between 1M and 1T2M devices: (a) when the two devices have a similar conductance window (G_{max}−G_{min}) and (b) when the two devices were operated under the same pulse conditions.

a 784 × 10 single-layer neural network instead of a multilayer neural network, as a universal method to implement the on-chip backpropagation algorithm in the hardware system has not been established. This single-layer can be implemented by using our designed synapse array, as shown in Figure 1a. To represent both positive and negative synaptic weight values, the two synaptic devices were grouped as one synapse unit. For the four test samples, as shown in Table 1, the recognition accuracy as a function of training samples was investigated (Figure S6 in the Supporting Information). Figure 7b shows the recognition accuracy results of the four test samples. While the 1M synaptic device has a poor accuracy of approximately 10% owing to its abrupt reset characteristics, the 2M1T synaptic device exhibits a greatly improved accuracy of approximately 90%.

CONCLUSIONS

In this study, we demonstrated a 1T2M synaptic device, its array structure, and its operation method for neuromorphic system applications. Amorphous IGZO was used for the switching layer of the memristor and as the channel material of the transistor. By using an XPS depth profile at each state, we investigated the switching mechanism of a Pd/IGZO/Si memristor. We observed that the proposed 1T2M synaptic device could improve the linearity and symmetry of conductance modulation. Furthermore, it could exhibit a wider total conductance window owing to the inherent current amplification of the transistor. Finally, we demonstrated that the 1T2M device can obtain better accuracy in pattern recognition applications. The proposed 1T2M device and its array structure will be a promising solution for the neuromorphic system. In particular, the IGZO-based 1T2M synaptic device could enable more functional system applications such as wearable electronics and large-area electronics.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.0c00499.

AFM (Atomic Force Microscopy) images of IGZO films; XPS peaks along with the depth of IGZO memristor; hysteresis, effective mobility, and subgap density-of-states of IGZO transistor; room-temperature state retention and read disturb of the IGZO memristors and transistors; and classification accuracy as a function of the number of trained samples (PDF)

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Author Contributions

D.H.K. conceived and designed the experiments. Y.K. analyzed the results and designed additional experiments. J.T.J conducted the device fabrication process, performed the electrical experiments, and wrote the manuscript. D.K. and W.S.C. conducted the device fabrication process and performed the electrical experiments. All the authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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