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Fabrication and characterization of Pt/Al2O3/Y2O3/In0.53Ga0.47As MOSFETs with low interface trap density

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In this work, we fabricated the In0.53Ga0.47As metal-oxide-semiconductor field-effect-transistors (MOSFETs) with a MOS interface of Y2O3/In0.53Ga0.47As and recessed gate structure. We investigated the interfacial properties of the gate stack and the junction characteristics of the fabricated MOSFETs. Low subthreshold slope (SS = 110 mV/dec), high on/off current ratio (Ion/Ioff = 106), and high effective mobility of 1600 cm2/V s were achieved in the MOSFETs at a sheet charge density (N_F) = 1.2 × 1011 cm−2. From the temperature dependence of I−V characteristics, the interface trap density was extracted to be Dit = 2.2 × 1011 cm−2 eV−1 with a negligible trap-assisted leakage current.

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InGaAs is the most prospective channel alternative for n-channel field effect transistors in future logic devices due to its high electron mobility and injection velocity.1,2 Recent advance in metal-oxide-semiconductor (MOS) interface control in high-k/InGaAs systems allows a low SS and high effective mobility, which are important to reduce VDD in VLSI circuits.3–5 In particular, the trivalent oxide has a better interfacial quality than the HfO2/InGaAs interface.6,7 Finally, we chose the Y2O3 gate dielectric because the k-value of Y2O3 (14–17.8) is higher than that of Al2O3 (9–10), which is typically used as an interfacial layer. Suzuki et al.8 reported a low equivalent oxide thickness (EOT) gate stack using the Al2O3 as an interfacial layer between InGaAs and HfO2 (higher-k material than Al2O3). Recent studies on InGaAs MOSFETs have used Al2O3/a higher-k gate dielectric for the gate stack with a thin EOT.9–11 For an ultimate EOT scaling, on the other hand, the k-value of the interfacial layer should also be scaled. Therefore, developing a higher-k interfacial layer than the dielectric constant of Al2O3 is quite important. However, the gate stack of Al2O3 has been studied widely than other high-k dielectrics. Although Chang et al.12 reported InGaAs MOSFETs with Y2O3, the extracted interface trap density (Dit) in InGaAs MOSFETs was quite high, resulting in high SS at a given EOT. We also reported InGaAs MOSFETs with low SS utilizing Y2O3 as a gate dielectric.13 However, the device structure was a bottom gate InGaAs-on-insulator, which remained for a feasibility study.

In this work, therefore, we investigated the interfacial properties of Y2O3/In0.53Ga0.47As by using In0.53Ga0.47As metal-oxide-semiconductor (MOS) capacitors. We also investigated the electrical performance and junction characteristics of top-gate In0.53Ga0.47As metal-oxide-semiconductor field-effect-transistors (MOSFETs) with Y2O3 as a gate dielectric and recessed gate structure. To investigate the MOS interface between the gate insulator (Y2O3) and In0.53Ga0.47As channel, we fabricated the MOS capacitors. The channel layers are 500-nm-thick n-In0.53Ga0.47As (doping concentration, N_D of approximately 1 × 1016 cm−3), which was grown on a highly doped n-InP (001) wafer with N_D ~ 1018 cm−3 by the metal organic chemical vapor deposition (MOCVD). After at ex-situ surface treatment of the III–V wafers with NH4OH and (NH4)2S solutions, a 10-nm-thick-Y2O3 layers were deposited on III–V layers by the electron beam (EB) evaporator. Then, 5-nm-thick-Al2O3 layers were deposited on Y2O3 layers by the atomic layer deposition (ALD). Finally, the gate was formed by the Pt (30 nm)/Au (70 nm) deposition.

To verify the effect of the post metallization annealing (PMA), MOS capacitors were annealed at several temperatures by the annealing chamber. Figure 1 shows a schematic image of the MOS capacitor and the multi-frequency C-V characteristics of the MOS capacitors annealed in N2 ambient at an annealing temperature of 250, 300, 350, and 400°C. As-deposited device showed poor C-V characteristics with a severe frequency dispersion. Annealed devices at 250 and 300°C showed a significant improvement of C-V characteristics compared with the as-deposited device in the frequency dispersion and steep capacitance change by gate voltage sweeping from the accumulation to the depletion stages. The MOS capacitor annealed at 350°C showed the steepest capacitance change and the smallest frequency dispersion. However, with annealed device at 400°C, C-V characteristics were slightly degraded at the bias range from the depletion to the inversion stages.

To quantitatively evaluate the C-V characteristics and interfacial quality, we extracted D_T(E) by the conductance

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method. We obtained the parallel conductance per unit area ($G_p$) from the measured equivalent circuit. We note that

$$G_p/\omega = C_ox - C_m$$

with $G_m$ as the measured conductance per unit area, $C_ox$ as the oxide capacitance per unit area, $\omega = 2\pi\nu$ as the angular frequency, and $C_m$ as the measured capacitance per unit area. Eq. (1) shows the fitted $G_p/\omega$ versus the frequency curve extracted by Eq. (1). We also considered the surface potential fluctuation (SPF) due to the non-uniformity of the oxide charge and the interface traps.\(^{14}\) Finally, we obtained the experimental $D_{it}(E)$ ranging from $10^{11}$ to $10^{12}$ cm\(^{-2}\)/eV considering the SPF. Annealed sample at 400°C has generally a higher $D_{it}$ than that at 350°C. Possible origin of this degradation is the Ga up-diffusion, which occurred with annealing at a high temperature of 400°C.\(^{15}\) The MOS capacitor annealed at 350°C had the lowest $D_{it}(E)$ among devices shown in Fig. 2(b). We found that the best annealing temperature to achieve a low $D_{it}$ is observed to be $T = 350°C$ and $D_{it} \sim 2 \times 10^{11}$ cm\(^{-2}\)/eV. This is quite low among any high-$k$/InGaAs interface and is comparable with that of reported high-$k$/InGaAs interface such as Y$_2$O$_3$/InGaAs and Al$_2$O$_3$/InGaAs. Also, the interfacial quality of Y$_2$O$_3$/InGaAs showed lower $D_{it}$ values than that of Al$_2$O$_3$/InGaAs as shown in Fig. 2(b).

Fig. 3(a) shows a schematic image of the device structure and fabrication process. To fabricate the recessed gate In$_{0.53}$Ga$_{0.47}$As MOSFETs, epitaxial layers were grown on semi-insulating (S. I) InP (001) wafer by the MOCVD process. The 50-nm-thick InP buffer layer ($N_A \sim 1 \times 10^{17}$ cm\(^{-3}\)) was grown on S. I. InP (001) wafer. The device layers were composed of 20-nm-thick In$_{0.53}$Ga$_{0.47}$As channel (unintentionally doped), 5-nm-thick InP etch stop (unintentionally doped), 50-nm-thick n$^+$ In$_{0.53}$Ga$_{0.47}$As contact layer ($N_D \sim 1 \times 10^{19}$ cm\(^{-3}\)) from the bottom side. In the first, device isolation was carried out by the mesa etching process. Then, n$^+$ In$_{0.53}$Ga$_{0.47}$As and InP were recessed in gate regions by citric acid and HCl solutions, respectively. Subsequently, it was cleaned by acetone, NH$_4$OH, and (NH$_4$)$_2$S solutions to remove the native oxide and to passivate the surface by sulfur(S) atoms. As a gate dielectric, 10-nm-thick Y$_2$O$_3$ and 5-nm-thick Al$_2$O$_3$ was deposited by EB evaporator and ALD, respectively. Here, Al$_2$O$_3$ was deposited for the step-coverance around the mesa to prevent the leakage current over the edge. The gate metal (Pt/Au) was formed by the EB evaporation, followed by the rapid thermal annealing (RTA) at 350°C for 1 min. in N$_2$ ambient. Finally, Ni was deposited for the S/D contacts.

![FIG. 1. C-V characteristics of Pt/Al$_2$O$_3$/Y$_2$O$_3$/n-In$_{0.53}$Ga$_{0.47}$As MOS capacitors at several frequencies (a) schematic image of MOS capacitors (b) as-deposited (c) after RTA at 250°C (d) 300°C (e) 350°C (f) 400°C for 30 min at N$_2$ ambient.](image1)

![FIG. 2. (a) The comparison of parallel conductance ($G_p/\omega$) versus frequency between as-deposited, RTA at 250, 300, 350, and 400°C at $E-E_i = 0.06$ eV (b) Energy distribution of $D_{it}(E)$, evaluated by the conductance method for Pt/Al$_2$O$_3$/Y$_2$O$_3$/n-In$_{0.53}$Ga$_{0.47}$As MOS capacitors with an annealing temperature.](image2)

![FIG. 3. (a) Schematic image of the final device structure and fabrication process of InGaAs MOSFETs (b) Cross-sectional TEM image of Y$_2$O$_3$/InGaAs interface.](image3)
transmission electron microscope (TEM) image of the fabricated Y2O3/In0.53Ga0.47As stack in Fig. 3(b) shows an abrupt interface between Y2O3 and In0.53Ga0.47As.

Electrical characterization was carried out for the fabricated In0.53Ga0.47As MOSFETs. Figs. 4(a) and 4(b) show the typical drain current (ID)-VGS (gate voltage) and IDVDS (drain voltage) characteristics of the In0.53Ga0.47As MOSFETs with a gate length (Lg) of 4 μm. Good ISGS-VGS curves were obtained with steep subthreshold slope (SS = 110 mV/dec) considering a thick equivalent oxide thickness (EOT) (~4.6 nm) of the device and a high on/off ratio (10^6). We obtained the gate current at least 4-orders lower than the drain current. Also, a clear current saturation was observed in the output characteristics.

To further characterize the electrical properties of the gate stack and the junction formation in the fabricated MOSFETs, we evaluated the effective mobility (μeff) and temperature dependence of I-V characteristics. We obtained μeff ~ 1600 cm^2/V·s at the sheet charge density (Nc) = 1.2 x 10^12 cm^-2 due to the good interfacial quality between Y2O3 and In0.53Ga0.47As. μeff values were obtained to be roughly two times higher than that of Si MOSFET all over the range of Nc as shown in Fig. 4(c). Our μeff value is comparable to that reported of the other group. Fig. 5(a) shows the temperature dependence of transfer curves of the In0.53Ga0.47As MOSFET with Lg = 4 μm at VDS = 0.05 V. To investigate the leakage current mechanism at the off-state, we evaluated the temperature-dependence of the off-state current (Ioff). Inset of Fig. 5(a) shows Ioff at several bias points as a function of 1/kT with kT as the average thermal energy. It was found that ln(Ioff) and 1/kT shows a linear relationship. From the slope of the plot in inset of Fig. 5(a), the activation energy (Eg) was extracted to be Eg ~ 0.37 eV which is close to a half of bandgap of In0.53Ga0.47As. Ioff behavior in our device that can be explained by the generation current (Igen) in PN junction, which can be expressed by

\[
I_{gen} = A \int_0^{W_d} q g_{ih} dx \equiv A \frac{q n_i}{2\tau_0} W_d \quad \text{with} \quad g_{ih} = \frac{n_i}{2\tau_0},
\]

where \(A\), \(n_i\), \(\tau_0\), and \(W_d\) as the effective junction area, the intrinsic carrier concentration, the excess carrier lifetime in the depletion region, and the depletion width, respectively. Since Igen is proportional to \(n_i\), an activation energy (Eg) of Ioff in PN junction dominated by Igen is extracted to be Eg = 2. This result indicates that the generation current is dominant in the S/D junction in the device at the off-state and the trap-assisted tunneling current is quite minor in the S/D junction. SS was monotonically decreased with decreasing the temperature as shown in Fig. 5(b). From the relationship between SS and temperature, \(D_a\) was extracted to be 2.2 x 10^{11} cm^-2·eV^-1, which is quite low among the reported \(D_a\) values of high-k/InGaAs interfaces. SS is expected to be further improved by scaling the EOT and reducing \(D_a\). Here, we assumed that the channel layer is fully depleted. \(C_{dep} = 6.11 \times 10^{-7} \text{F/cm}^2\), \(\varepsilon_{InGaAs} = 13.8\varepsilon_0\).

Finally, in this work, we obtained \(SS = 110 \text{ mV/dec}\) and \(D_a\) of approximately 2.2 x 10^{11} cm^-2·eV^-1. We found that \(D_a\) in the MOSFETs with the MOS interface of Y2O3/In0.53Ga0.47As. By scaling down of the EOT and channel thickness, it is expected to achieve \(SS \sim 60 \text{ mV/dec}\) with the Al2O3/Y2O3/In0.53Ga0.47As gate stack. We believe that our work with thick EOT is also quite meaningful as a feasibility study. Also, further improvements of the electrical properties in In0.53Ga0.47As MOSFETs are expected through further process optimization such as EOT and gate length scaling as well as a thin body structure as a future work.

In this study, we fabricated In0.53Ga0.47As MOSFETs with a MOS interface of Y2O3/In0.53Ga0.47As and a recessed gate structure. We investigated the electrical properties of fabricated In0.53Ga0.47As MOSFETs and achieved low \(SS = 110 \text{ mV/dec}\) and high on/off ratio (10^6). The effective channel carrier mobility \(\mu_{eff}\) was also as high as 1600 cm^2/V·s at \(n_i = 1.2 \times 10^{12} \text{ cm}^{-2}\), which is much higher than the conventional Si MOSFETs. From the temperature dependence of
I–V characteristics, we obtained $D_{it} = 2.2 \times 10^{11} \text{cm}^{-2} \cdot \text{eV}^{-1}$ and a negligible trap-assisted leakage current in the S/D junction. These results strongly suggest that Y$_2$O$_3$ is a promising dielectric interlayer for extremely low EOT gate stack in In$_{0.53}$Ga$_{0.47}$As MOSFETs.

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