Semiconductor Science and Technology

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Semiconductor Science and Technology

Semicond. Sci. Technol. **35** (2020) 03LT01 (5pp)

https://doi.org/10.1088/1361-6641/ab6bab

Letter

Design study of the gate-all-around silicon nanosheet MOSFETs

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Received 7 July 2019, revised 26 November 2019
Accepted for publication 14 January 2020
Published 11 February 2020

Abstract

The gate-all-around (GAA) silicon nanosheet (SiNS) metal-oxide-semiconductor field-effect transistor (MOSFET) structures have been recognized as excellent candidates to achieve improved power performance and area scaling compared to the current FinFET technologies. Specifically, SiNS structures provide high drive currents due to wide effective channel width (W_{eff}) while maintaining short-channel control. In this paper, we fabricate a GAA SiNS MOSFET fully surrounded by a gate with a gate length (L_G) of 22 nm, a SiNS width (W_{NS}) of 23 nm, and SiNS thickness (T_{NS}) of 6 nm. In addition, the fabricated GAA SiNS MOSFETs were evaluated for electrostatic characteristics and short-channel effects (SCEs) according to various channel length and width dimensions. We confirmed that the GAA SiNS MOSFET showed similar short-channel controllability regardless of W_{NS} due to the extremely thin T_{NS}. In addition, we analyzed SCEs of GAA SiNS MOSFETs with different T_{NS} through simulation.

Keywords: silicon nanosheet, gate all around, MOSFET, short-channel effects, effective width

(Some figures may appear in colour only in the online journal)

1. Introduction

During the last decade, many new technologies such as strained-silicon, high-κmetal gate, and three-dimensional (3D) device structures have been developed to improve device performance and reduce short-channel effects (SCEs) [1–4]. Fin field-effect transistors (FinFETs), as 3D devices, have successfully enabled continuous technology scaling from planar metal-oxide-semiconductor FETs (MOSFETs) by improving gate-to-channel control [5, 6]. However, FinFETs are currently facing many challenges in terms of device performance, layout, and cost for further scaling. Therefore, the gate-all-around (GAA) silicon (Si) nanowire MOSFETs with superior channel potential controllability and high current drivability are expected to solve the aforementioned problems and are considered to be the ultimate scaled transistor structure [7–10]. One of the possible limiting factors in the GAA Si nanowire MOSFETs is inherently the small effective channel width (W_{eff}), i.e. the channel perimeter, resulting in low drive currents, but this can be compensated by stacking multiple nanowires. However, another drawback of increasing the parasitic capacitance component is raised inevitably [11].

Recently, GAA Si nanosheet (SiNS) MOSFETs have been introduced to continue scaling [12–15]. The SiNS structure provides higher drive current, compared to the FinFETs and GAA SiNW MOSFETs, because the W_{eff} is enlarged and not limited. Therefore, this feature gives more freedom to the device design options. However, the enlarged W_{eff} might simultaneously affect electrostatics as well as drive current. Hence, we need to study the influence of the SiNS

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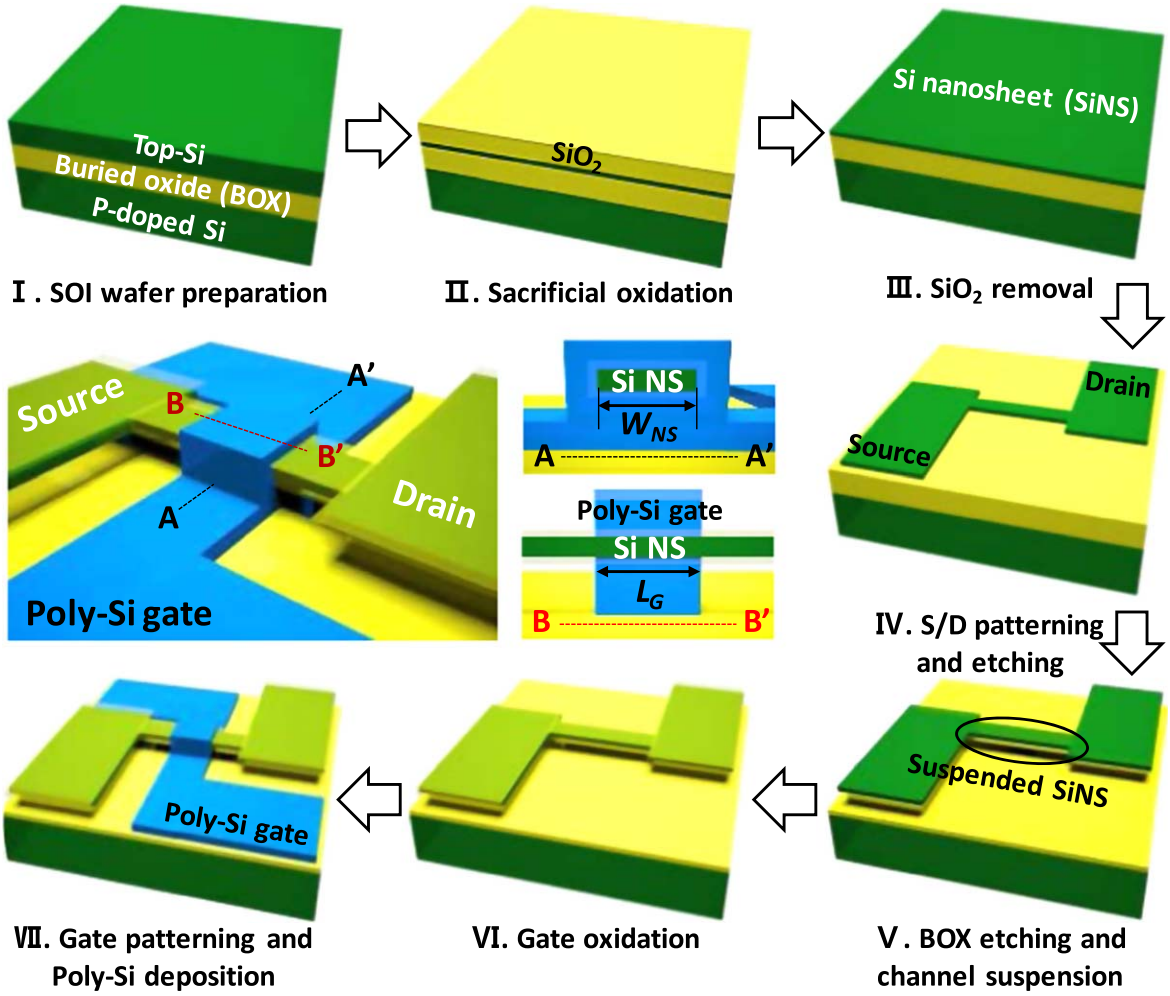

Figure 1. Process flow of the horizontal GAA SiNS MOSFETs (I) preparing SOI wafer by first cleaning; (II) sacrificial oxidation to shrink down top-Si; (III) thermal oxide (SiO_2) removal with diluted HF solution; (IV) SiNS patterning and etching for active channel and S/D formation; (V) BOX etching with diluted HF solution for SiNS suspensions; (VI) size reduction of SiNS channel and gate oxide formation by thermal oxidation; (VII) n-doped poly-Si deposition and patterning to define the L_G, followed by S/D doping with As. The middle panel shows a schematic cross-section in W_{NS} and L_G direction of the completed GAA SiNS MOSFET.

widths on the electrostatic control. In this work, we fabricated the GAA SiNS MOSFET with various gate lengths (L_G) and NS widths (W_{NS}) on the 8 inch SOI-wafer to explore the electrostatics at a dc level. We chose the SiNS thickness of 6 nm because it has been reported that the comparable electrostatic control to FinFETs can be achieved by reducing NS thickness to 5 nm. We also investigated the short-channel controls through the technology computer-aided design (TCAD) simulations to assess the fabricated devices and evaluate device electrostatics in the GAA SiNS MOSFETs with various physical parameters.

2. Measurement results and discussion

Figure 1 illustrates the details of the fabrication processes and shows a cross-sectional schematic diagram of the channel length and width direction of the GAA SiNS MOSFET. The fabrication process started on the p-type (100) SOI wafer with 145 nm thick top Si and 400 nm thick buried oxide (BOX). First, the thickness of the top Si (T_{NS}) was thinned to 20 nm through iterative wet oxidation processes and removal of formed thermal oxide. This process is a preliminary task for the efficient process of SiNSs. Next, the KrF scanner photolithography process using 0.18 μm technology was employed to define the SiNS. To achieve the minimum device feature size of the SiNS, the width of the patterned photoresist (PR) was reduced to 40 nm through a partial ashing process using an oxygen plasma. The BOX was then wet-etched with diluted HF solution to suspend the SiNS channel. Then, a sacrificial oxidation process was performed to alleviate the etching damage and to further reduce the dimensions of the suspended SiNS channel. As a result, the W_{NS} and T_{NS} were simultaneously reduced from 40 to 20 nm and from 20 to 10 nm, respectively. After wet-etching the sacrificial oxide, thermal oxidation with a thickness (T_{ox}) of 5 nm was performed to form a gate dielectric (SiO_2) such that the final T_{NS} was scaled down to 6 nm. Then, a highly n-doped poly-Si layer was deposited to surround the SiNSs for the gate electrode and the high-density plasma oxide (SiO_2) was deposited

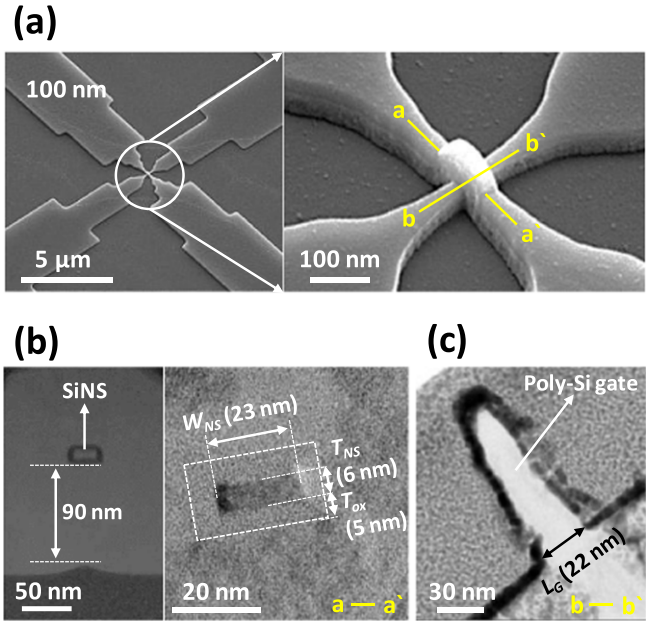

Figure 2. (a) Tilted SEM image of GAA SiNS MOSFET fully surrounded by poly-Si gate. (b) Cross-sectional TEM images along W_{NS} and (c) L_G direction of GAA SiNS MOSFET. The poly-Si gate is entirely surrounding the SiNS channel. The suspended distance is approximately 90 nm and T_{OX} is 5 nm. The SiNS dimension consist of W_{NS} of 23 nm, L_G of 22 nm, and T_{NS} of 6 nm.

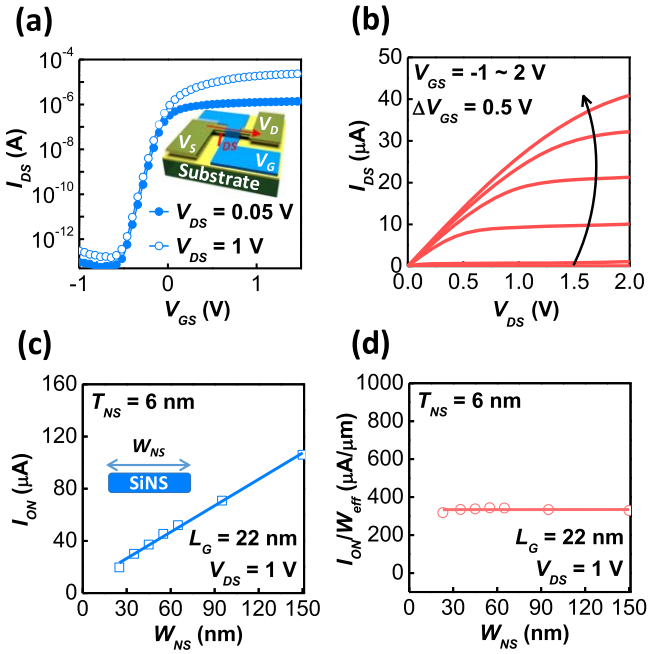

Figure 3. (a) Transfer characteristics ($I_{DS} - V_{GS}$) and (b) output characteristics of GAA SiNS MOSFET with L_G of 22 nm, W_{NS} of 23 nm, and T_{NS} of 6 nm. (c) The on-state current (I_{ON}) and (d) I_{ON} normalized per channel perimeter (W_{eff}) of the GAA SiNS MOSFETs with an L_G of 22 nm and a T_{NS} of 6 nm.

as a hard mask (HD) by a chemical vapor deposition method. For the gate patterning, the hard mask trimming process was employed in company with the PR ashing processes described above, for further reduction of the channel length. After the gate patterning, the source and drain (S/D) were doped with arsenic (As), and the dopants were activated. Finally, hydrogen-forming gas annealing with a mixture of H_2 and N_2 gases was applied for 30 min. The W_{NS} and L_G values in the fabricated devices ranged from approximately 20–150 nm and from 20 to 860 nm, respectively.

Figure 2(a) shows the scanning electron microscope images of the fabricated GAA SiNS MOSFET. The cross-sectional transmission electron microscope (TEM) images in the W_{NS} and L_G direction are also shown in figures 2(b) and (c). The TEM image clearly shows that 6 nm thick suspended SiNS is formed, and the gate oxide is entirely wrapped around the SiNS channel. The suspended distance between SiNS and BOX is approximately 90 nm.

The transfer and output characteristics (i.e. drain current, I_{DS} versus gate voltage, V_{GS} and I_{DS} versus drain voltage, V_{DS}) of the representative GAA SiNS MOSFET with W_{NS} of 23 nm, L_G of 22 nm, T_{NS} of 6 nm, and T_{ox} of 5 nm at different V_{DS} values of 0.05 and 1 V are shown in figures 3(a) and (b). The measured GAA SiNS MOSFET showed a subthreshold slope (SS) of 68 mV/dec, a transconductance (g_m) of 2.6 μS, and a drain-induced barrier lowering (DIBL) of 37.8 mV V^{-1}. Importantly, the on-state current (I_{ON}) of 318 $\mu A\ \mu m^{-1}$, which was normalized by W_{eff} = 58 nm (i.e. $W_{eff} = 2 \times W_{NS} + 2 \times T_{NS}$) was obtained at $V_{GS} - V_{T,sat} = 1$ V and $V_{DS} = 1$ V, indicating that I_{ON} in our device shows higher drive current values compared to previously reported GAA silicon nanowire MOSFETs due to enlarged W_{eff} without sacrificing the other performance aspects [4, 16–18]. In addition, the certain kink effect was not observed in the output characteristics, which confirms that the devices were fully depleted, and there are no sharp corners on the SiNS owing to the sacrificial oxidation during the processes. These electrical performances are expected to be further enhanced by reduction of equivalent oxide thickness and S/D optimization.

Table 1. Summary of the parameters used in the TCAD simulation.

Parameters	Value
Gate oxide thickness (T_{ox})	5 nm
Gate oxide dielectric constant	3.9
Gate length (L_G)	22–860 nm
Suspended distance	90 nm
Nanosheet thickness (T_{NS})	3–20 nm
Nanosheet width (W_{NS})	23 nm, 150 nm
Channel doping concentration	1×10^{15} /cm^3
n^+ S/D, gate doping concentration	1×10^{20} /cm^3

Figure 3(c) shows that the I_{ON} is generally decreasing when reducing the W_{NS} for the fabricated GAA SiNS MOSFET with an L_G of 22 nm, and the normalized I_{ON} by W_{eff}, i.e. I_{ON}/W_{eff}, of the GAA SiNS MOSFETs is shown in figure 3(d). Generally, in the FinFET, as the Fin width increases, the normalized I_{ON} value deteriorates due to the channel region which is not controlled by the V_{GS} bias [12, 19]. However, in the GAA SiNS MOSFET, the normalized I_{ON} value is maintained even as the W_{NS} increases, which is evidence that the gate is well wrapped around the entire SiNS channel and the controllability of the channel

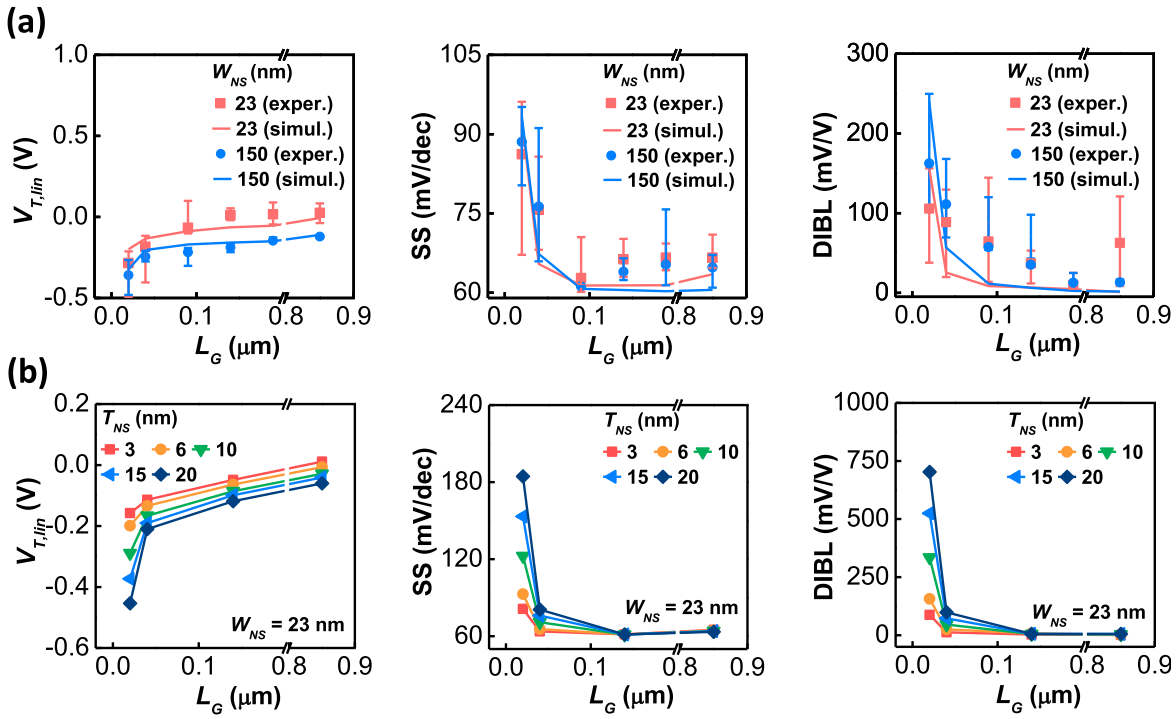

Figure 4. $V_{T,lin}$, SS, and DIBL as a function of L_G with different W_{NS} of 23 nm and 150 nm; (b) $V_{T,lin}$, SS, and DIBL as a function of L_G with various T_{NS} (3, 6, 10, 15, and 20 nm) in GAA SiNS MOSFETs.

potential is superior due to the thin T_{NS} thickness. Therefore, the GAA SiNS MOSFET exhibits the stable current control and higher drive current even at wider W_{NS} and provides more broad options to improve the drive current by choosing an appropriate W_{NS} compared with other devices.

In order to evaluate the fabricated devices, we investigated the SCEs through Synopsys Sentaurus TCAD simulations. Regarding the carrier transport model, we used a hydrodynamic model with quantum correction, which is widely used model for simulating FinFETs and GAA MOSFETs [19, 20]. Detailed device parameters are summarized in table 1. As shown in figure 4(a), we confirmed the L_G dependence of key SCE parameters such as $V_{T,lin}$, DIBL and SS in undoped body SiNS GAA MOSFETs with small W_{NS} of 23 nm and large W_{NS} of 150 nm through experiments (symbols) and TCAD simulations (lines) at T_{NS} of 6 nm. As a result, $V_{T,lin}$, SS, and DIBL were extracted with similar values regardless of W_{NS} for both experiments and simulation. Increasing the channel width in FinFETs and GAA MOSFETs with thick gate insulators or channels is well known to be vulnerable to SCEs [21–23]. However, since the T_{NS} of the fabricated GAA SiNS MOSFETs is extremely thin (6 nm), the channel potential is effectively controlled by the V_{GS} regardless of W_{NS}. Nevertheless, we need to make the T_{NS} thinner for continuous device scaling and high device performance. As data that can support the above, figure 4(b) shows simulation results of SCE parameters ($V_{T,lin}$, SS, and DIBL) for various T_{NS} in a GAA SiNS MOSFET with a 23 nm W_{NS}. The inset images in figure 4(b) show the SCE parameters magnified in the short L_G. Overall, SCEs were enhanced by improved gate-to-channel control in GAA SiNS MOSFETs with thinner T_{NS}. Although we analyzed the electrostatic characteristics and SCEs in single layer GAA SiNS MOSFETs, we will develop a further reduced T_{NS} device and discuss parasitic capacitance in a multilayer GAA SiNS MOSFETs.

3. Conclusions

A 20 nm scale GAA SiNS MOSFET implemented on an SOI substrate was demonstrated using a top-down manufacturing method. In particular, the proposed GAA SiNS MOSFETs formed extremely thin SiNS channels with a T_{NS} of 6 nm using PR ashing technology and sacrificial oxidation that are current CMOS-compatible technologies. We evaluated electrical performance in fabricated GAA SiNS MOSFETs and showed high drive current, high on/off ratio, and high device yield. Notably, our GAA SiNS MOSFETs observed similar short-channel controllability down to the L_G of 20 nm regardless of W_{NS} due to extremely thin T_{NS}. We also predicted from the simulation studies that GAA SiNS MOSFETs with thinner T_{NS} could achieve high performance and continuous device scaling. That is, further work is required to investigate SCEs in multilayer GAA SiNS MOSFETs with T_{NS} less than 5 nm.

Acknowledgments

This work was supported by the National Research Foundation (NRF) of Korea under grants 2016R1A5A1012966 and

2019R1A2B5B01069988 and by the Future Semiconductor Device Technology Development Program (Grant 10067739) funded by MOTIE (Ministry of Trade, Industry & Energy) and KSRC (Korea Semiconductor Research Consortium).

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